The FOSSi Foundation.

Can we do an open source chip design in 45 minutes?

Philipp Wagner
FOSDEM 2023

Yes.

Terms and conditions apply. Sit through this talk for details.

Our Agenda

- The technology: tools & processes to build an open source chip.
- The community: how we're working together.
- The future.

About Philipp

lowRISC

opentitan

ocotb

open source initiative

philipp@fossi-foundation.org
@imphil on GitHub
@MrImphil on Twitter

About FOSSi Foundation

The FOSSi Foundation exists to promote and protect the open source silicon chip movement. It actively encourages the community's growth and is helping to maintain the open spirit of the movement, through events, educational programmes and working groups. With an international membership of experts from academia and industry, it supports new open source initiatives and collaborations – offering free advice to governments and policy makers, corporations, academics and hobbyists. As a not-for profit organisation, the foundation is independent of any commercial interests and acts as a steward in support of open source projects which broadly benefit the open source silicon community. FOSSi is an acronym for Free and Open Source Silicon.

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Technology

How to build a chip?

Implement the chip's functionality

Realize this functionality in the physical world

Logic

Physics

Frontend

Program the chip's functionality.

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Just like programming

“Programming languages”	“All the other stuff”
High-Level Synthesis (HLS)	Test Frameworks
High-Level Languages	Build tools
SystemVerilog and VHDL	Developer productivity
Netlist	Simulators

Hardware description

- **(System)Verilog**
- **VHDL**
- **BlueSpec (Verilog/Haskell)**
- **Python-based**
  - Migen
  - Amaranth HDL
  - MyHDL
- **Based on functional programming languages**
  - Spinal-HDL (Scala)
  - Chisel (Scala)
  - Clash (Haskell)
- **CIRCT: LLVM**

Reuse and integrate

- LiteX
- (OpenCores)
- …

What can we do with a logic design?

- Verify it
- Document it
- Make it look pretty
- Simulate it
- Run it on an FPGA

Simulate it

GHDL

NVC

VERILATOR

Verification frameworks

SymbiYosys

Build and run

- FuseSoC and Edalize
- VUnit
- bazel_rules_hdl
- HDLMake
- …

Developer productivity

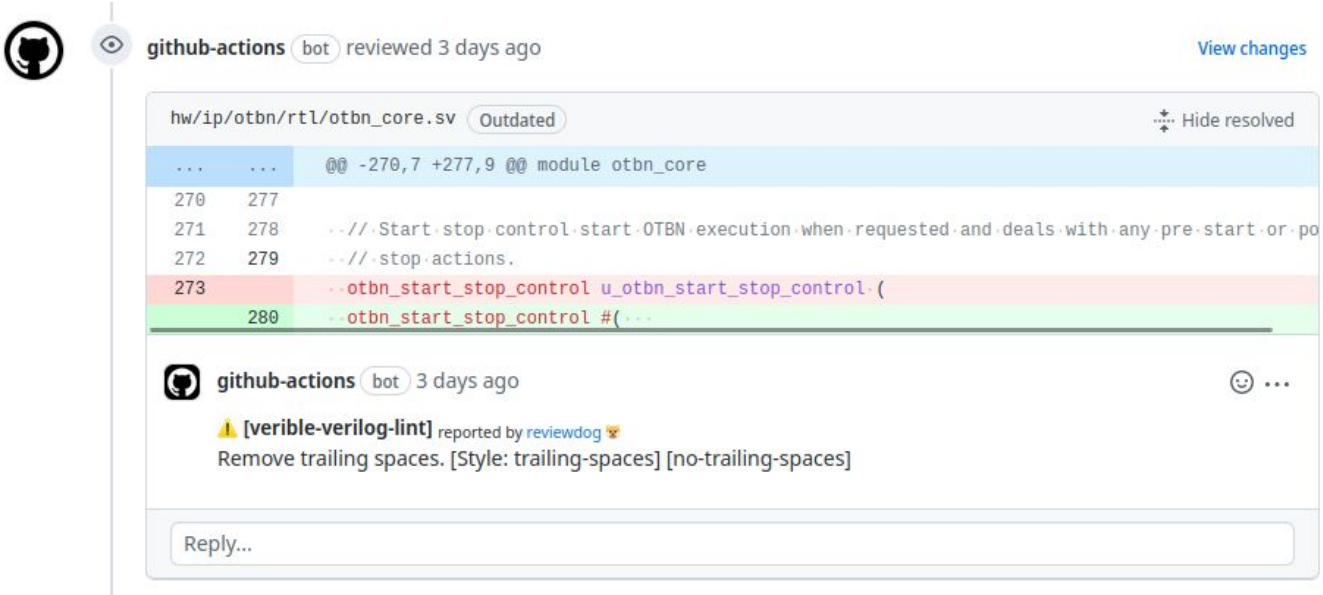
- **Verible: lint, formatter, code indexer, language server, and more**
  - Formatting based mostly on the lowRISC SV Style Guide
- **Verilator lint**
- **VHDL Style Guide (VSG)**
- **…**

Verilator lint

```
assign id_to_ping_d = (lfsr_state[PING_CNT_DW +: IdDw] >= NAlerts) ?
                      lfsr_state[PING_CNT_DW +: IdDw] - NAlerts    :
                      lfsr_state[PING_CNT_DW +: IdDw];
```

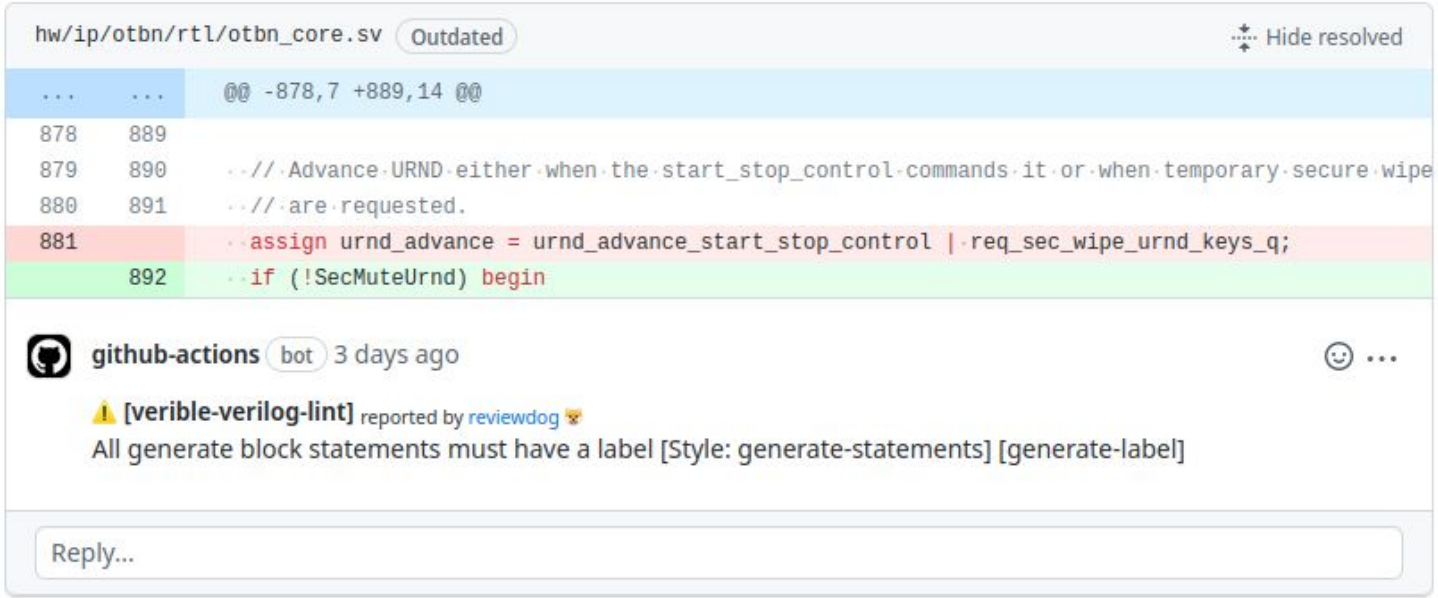
```
%Warning-WIDTH: ../src/lowrisc_ip_alert_handler_component_0.1/rtl/alert_handler_ping_timer.sv:131:58:
Operator GTE expects 32 bits on the LHS, but LHS's SEL generates 7 bits.

%Warning-WIDTH: ../src/lowrisc_ip_alert_handler_component_0.1/rtl/alert_handler_ping_timer.sv:132:57:
Operator SUB expects 32 bits on the LHS, but LHS's SEL generates 7 bits.

%Warning-WIDTH: ../src/lowrisc_ip_alert_handler_component_0.1/rtl/alert_handler_ping_timer.sv:131:70:
Operator COND expects 32 bits on the Conditional False, but Conditional False's SEL generates 7 bits.

%Warning-WIDTH: ../src/lowrisc_ip_alert_handler_component_0.1/rtl/alert_handler_ping_timer.sv:131:23:
Operator ASSIGNW expects 7 bits on the Assign RHS, but Assign RHS's COND generates 32 bits.
```

Automate reviews with Verible lint



Screenshot from https://github.com/lowRISC/opentitan/pull/17195

Automate reviews with Verible lint



Screenshot from https://github.com/lowRISC/opentitan/pull/17195

Summary

- The frontend is doing great.
- If we could only avoid re-inventing Verilog parsing.

Backend

Run your design on an FPGA

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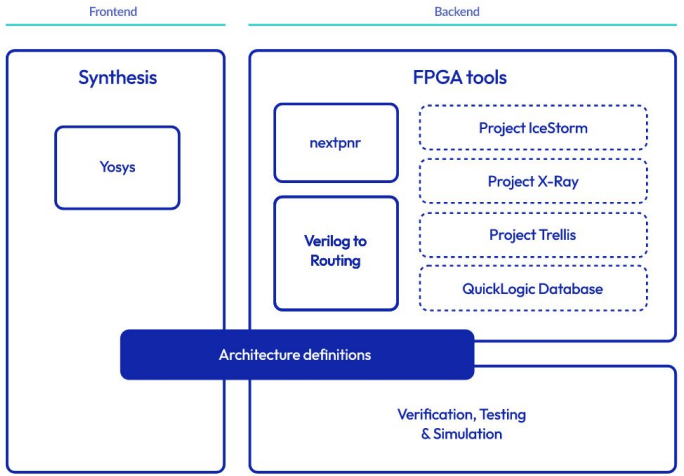
Run it on an FPGA

F4FPGA (formerly SymbiFlow)

F4PGA

	Project Icestorm	Project Trellis	Project X-Ray	QuickLogic Database
Basic Tiles:	✓	✓	✓	✓
- Logic	✓	✓	✓	✓
- Block RAM	✓	✓	✓	✓
Advanced Tiles:	✓	✓	✓	✓
- DSP	✓	✓	✗	✓
- Hard Blocks	✓	✓	✗	✓
- Clock Tiles	✓	✓	✓	✓
- IO Tiles	✓	✓	✓	✓
Routing:	✓	✓	✓	✓
- Logic	✓	✓	✓	✓
- Clock	✓	✓	✓	✓




HOGWARTS SCHOOL OF

Open Source Silicon

Si

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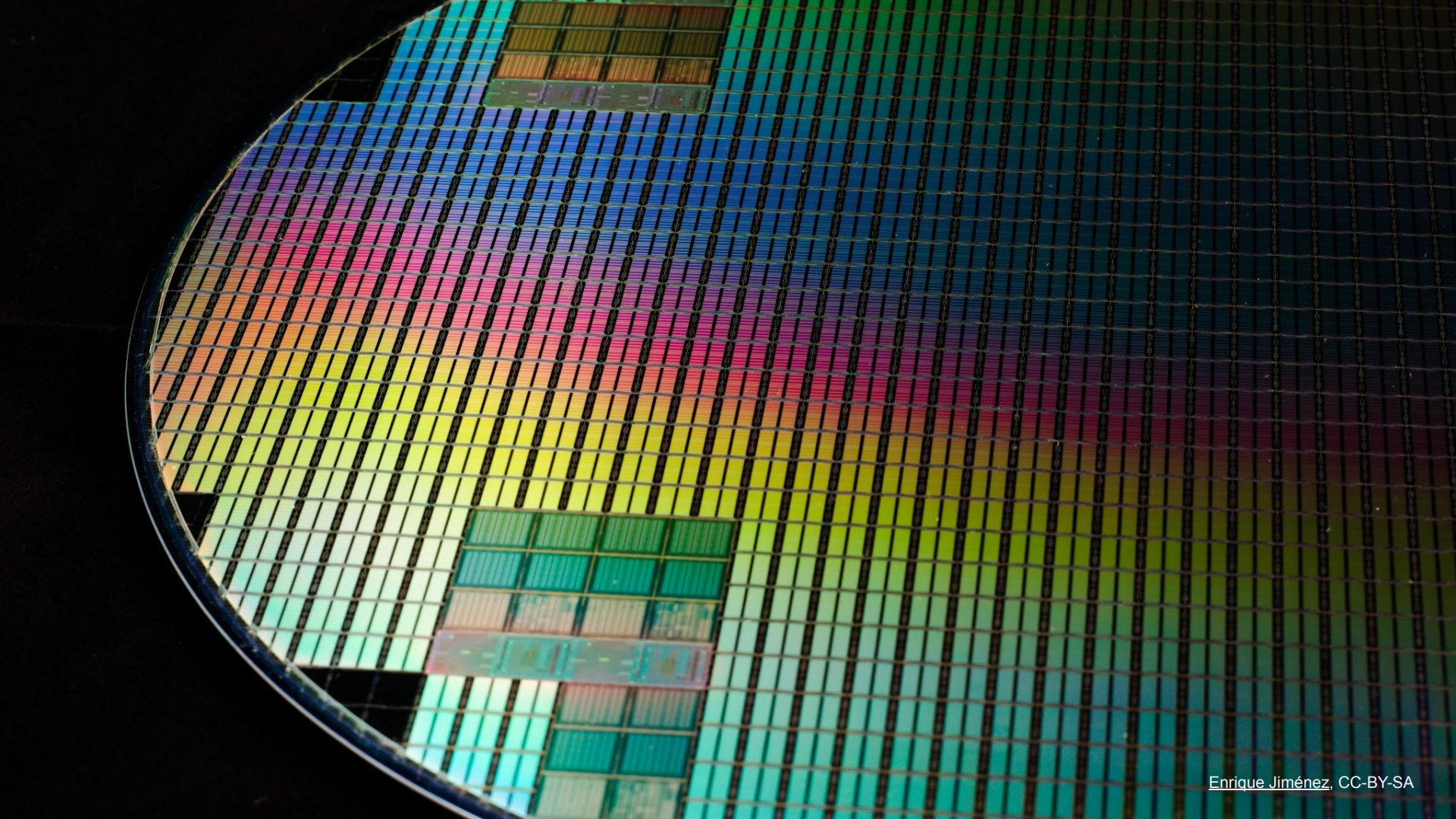

Enrique Jiménez, CC-BY-SA

Backend

Design the physical implementation

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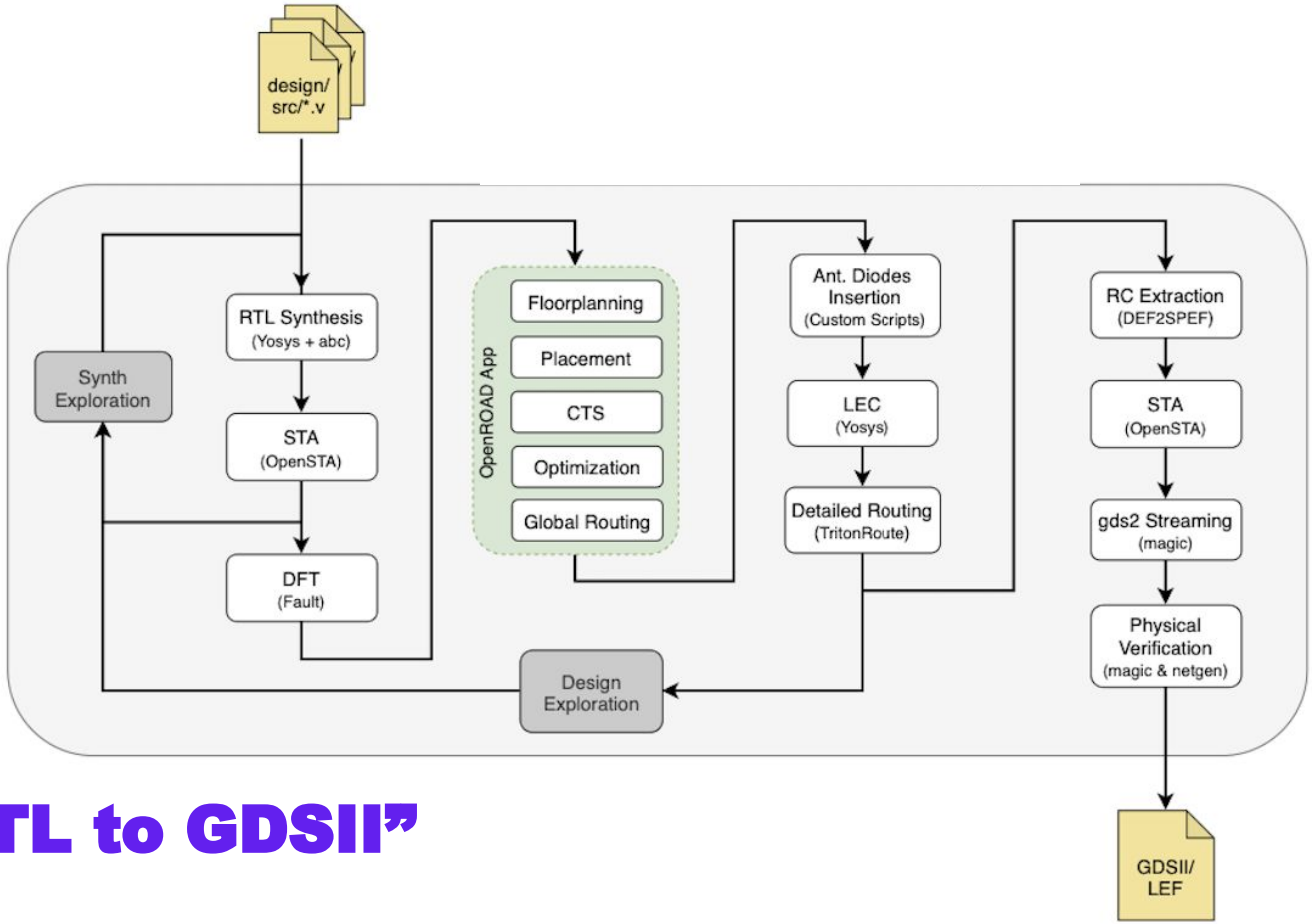
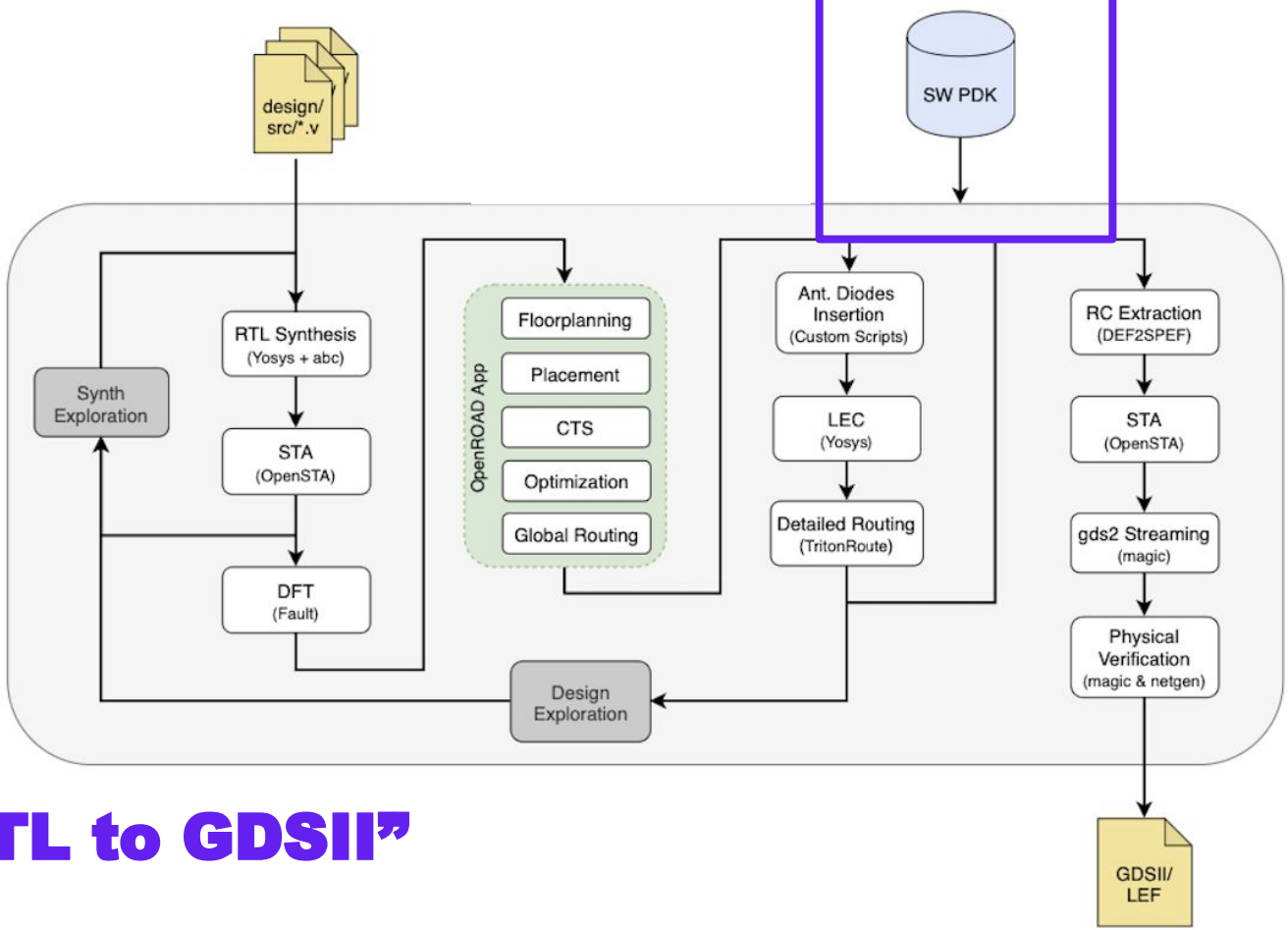

design/
src/*.v
RTL Synthesis
(Yosys + abc)
Synth
Exploration
STA
(OpenSTA)
DFT
(Fault)
OpenROAD App
Floorplanning
Placement
CTS
Optimization
Global Routing
Ant. Diodes
Insertion
(Custom Scripts)
LEC
(Yosys)
Detailed Routing
(TritonRoute)
RC Extraction
(DEF2SPEF)
STA
(OpenSTA)
gds2 Streaming
(magic)
Physical
Verification
(magic & netgen)
Design
Exploration
GDSII/
LEF

"RTL to GDSII"


design/
src/*.v
SW PDK
RTL Synthesis
(Yosys + abc)
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STA
(OpenSTA)
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(Fault)
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gds2 Streaming
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Verification
(magic & netgen)
Design
Exploration
GDSII/
LEF

“RTL to GDSII”

03

The Process Design Kit (PDK)

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The Design Kit

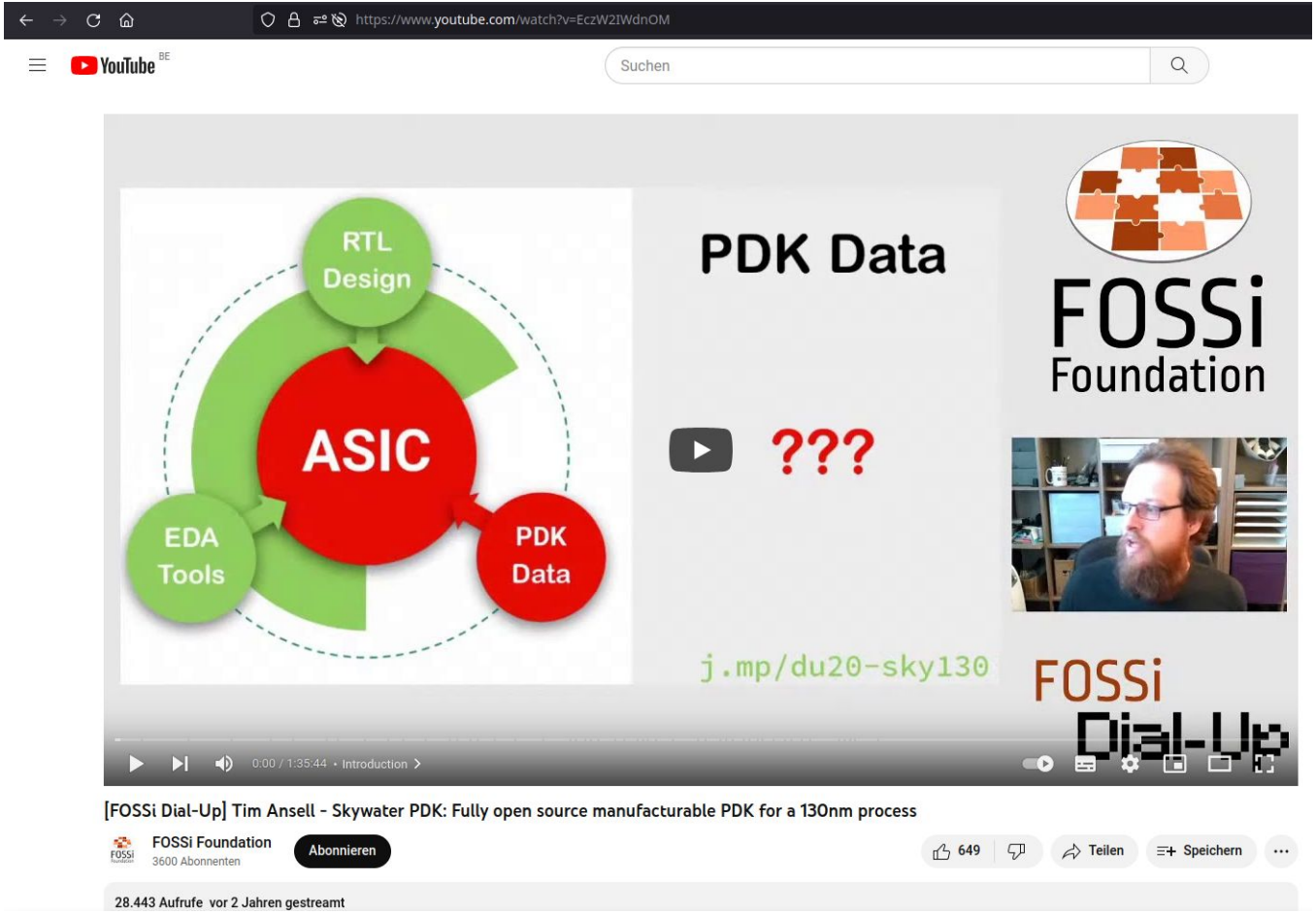
- standard cell libraries, design rules, electrical parameters, ...
- get it from the foundry
- bad: requires pretty tough NDA
- good: it's usually for free (again, as in beer)

"The ASIC Check": Results

- Hobbyist-Accessibility-Score: 0.1/5
- FOSS score: 1/5
- Fun score: 1-5/5
- Satisfaction score: 10/5

let's do it anyways?

lowRISC
OPEN TO THE CORE



Screenshot from https://www.youtube.com/watch?v=EczW2IWdnOM


SCALEO 600 X
AMD Athlon™ XP Prozessor 1700+
mit QuantiSpeed™ Technologie
266 MHz-Front-SideBus
Mainboard VIA KT 266
verfügbare Slots 3x PCI, 1x CNR, 3x AGP
AMD Athlon™ XP-Prozessor 1700+
mit QuantiSpeed™ Technologie
256 MB DDR-RAM Arbeitsspeicher
Doppelte-Daten-Rate
(Erweiterbar bis max. 1,536 GB)
40 GB Festplatte (5.400 U/min)
Praktische Frontanschlüsse:
• 2xUSB • Audio in • Audio out
16-fach-DVD
48-fach-CD-ROM-Laufwerk
Video Grafik-Karte VGA
64 MB nVIDIA Geforce 2MX 400
mit TV-Out
16x/12x/40x CD-Brenner
16-fach schreiben
12-fach wiederbeschreiben
40-fach lesen
TT Solo 1 SL
PCI Sound-Karte mit Wavetable-Software
• VSpace™ 3D Effekt • SoundBlaster/PRO kompatibel
3,5" 1,44 MB Diskettenlaufwerk
2 JAHRE GARANTIE
• 2 Jahre auf PC/
Hardware-Komponenten
• 48-h-Vor-Ort-Service
• Service-Hotline ist
365 Tage erreichbar
56 K internes Modem
mit Fax- und Anrufbeantworter-Funktion
1x 51/4" freie Einschübe,
4 USB-Schnittstellen (2 vorne/2 hinten)
Inklusive Bedienungsanleitung und sämtlichen Anschluss-Kabeln
Mit umfangreichem Software-Angebot
MULTIMEDIA-Tastatur:
Inklusive auswechselbaren Handballen-Auflagen in 3 Farben
3-Tasten-Wheel-Mouse:
Inklusive Mouse-Pad
Weitere Informationen erhalten Sie in unserem Handzettel
1998,–


ALDI informiert
...ab Mittwoch, 26. März
Der MEDION Titanium MD 8008 mit Intel® Pentium® 4 Prozessor 2,6 GHz
Einmalig
Der neue ALDI-PCXL Titanium MD 8008 von MEDION
intel inside
pentium 4
ECHTE 2,6 GHz
512KB Second Level Cache • Motherboard mit 3PCI-Steckplätzen • Grafik aufrüstbar durch AGP 8x Steckplatz • Arbeitsspeicher aufrüstbar durch einen freien Speichersteckplatz
Sony DVD-ROM 16x
Seagate 160 GB Festplattenkapazität Superschnell 7200 U/Min Ultra ATA100 Interface
ATI ATIRadeon9600TX 128MB DDR SDRAM 540 MHz Volle Hardwareunterstützung für DirectX 9
Samsung 512 MB DDR 333MHz Arbeitsspeicher 1 Modul - erweiterbar (max. 2 GB)
MEDION Stereo TV-, FM-Radio Karte Geeignet für: Kabel- und Antennenempfang (terrestrisch)
MEDION Funkfernbedienung Zur bequemen Steuerung der DVD-, TV-, Video-, CD-, Radio- und Fotofunktionen (Medion Power Cinema)
Firewire 3x Firewire/IEEE 1394 1 vorne · 2 hinten
DOLBY DIGITAL 6-Kanal Heimkinoton für das digitale Heimkinoerlebnis
DSL & Network Ready Netzwerkcontroller on board Fast Ethernet 10/100 MBit
MEDION 5 x USB 2.0 3 vorne · 2 hinten
MEDION 56K V.9x PCI Daten Fax Modem inkl. Faxsoftware und Telefon-Anschlußkabel OEM Version
Microsoft IntelliMaus® OEM Version
MEDION PS/2-Tastatur mit nützlichen Zusatztasten
DVD RW
DVD ROM
CONNECTXL
MEDION
Der Testsieger**
Pioneer DVD-Brenner + CD-Brenner in einem Gerät
4x DVD-R 2x DVD-RW
** Computerbild 26/2002. Unter 8 DVD-Brennern im Test schnitt der Pioneer Brenner als bestes Gerät mit der Note 2,8 ab.
15 IN 1
DVDs und Video-CDs brennen
Digitaler Videorecorder
Zeitversetztes Fernsehen
Riesige Festplattenkapazität
Musik-CDs kopieren und erstellen
Heimkinoton für Video-DVDs
Mehrere Bildschirme anschließen
Bilder in Kinoqualität
Radio über Internet und Antenne
Lesegerät für digitale Fotos
Praktische Anschlüsse vorne
Besonders leise durch AIR-XL
Internet über 56k Datenfax-Modem
Riesiges Software-Paket
Optimal spielen, arbeiten und...
Der MultiMedia Internet PC inklusive:
DVD-Brenner / CD-Brenner • Fernbedienung • Office PC • High Performance Spiele Center • DVD Dolby Digital Home Cinema System • Stereo TV Tuner • Stereo Radio Tuner • Digitaler Videorecorder mit Time Shift Funktion • Multifunktions Kopier Center • Netzwerk Power Station • Multifunktions MP3 Maschine • Music Juke Box Video / Bildbearbeitungsmaschine • Kommunikationscenter
1.179,–*
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www.medion.de | your digital future is now
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efabless.com

Startups Universities Research Login or Signup

Make Your Own Chips for Free

Design and fabricate your own open-source design for free with the Open MPW Program

MPW-7 Submission Deadline is September 12

Welcome to the Efabless Open MPW Program

efabless.com

The shuttle provides opportunities for designers to

The future of Intel's manufacturing processes

by Anand Lal Shimpi on December 11, 2000 1:23 AM EST

“Realistically speaking, we should be able to see **NetBurst based processors reach somewhere between 8 – 10GHz in the next five years** before the architecture is replaced yet again. Reaching 2GHz isn’t much of a milestone, however reaching 8 – 10GHz begins to make things much more exciting than they are today. Obviously this 8 – 10GHz clock range would be based on Intel’s 0.07-micron process that is forecasted to debut in 2005. These processors will run at less than 1 volt, 0.85v being the current estimate.”

https://www.anandtech.com/show/680/6

Installing EDA tools has never been easier

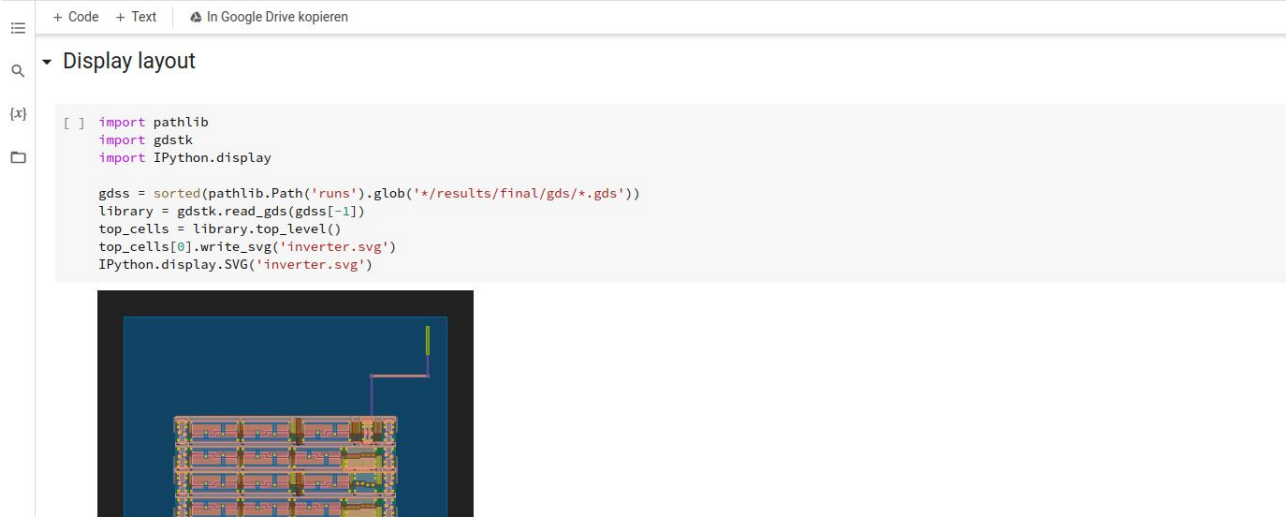
```
$ git clone https://github.com/The-OpenROAD-Project/OpenLane
$ cd OpenLane
$ make
$ make test
$ make mount
```

Additionally used for demo: https://github.com/mattvenn/openlane_summary

OpenLane demo

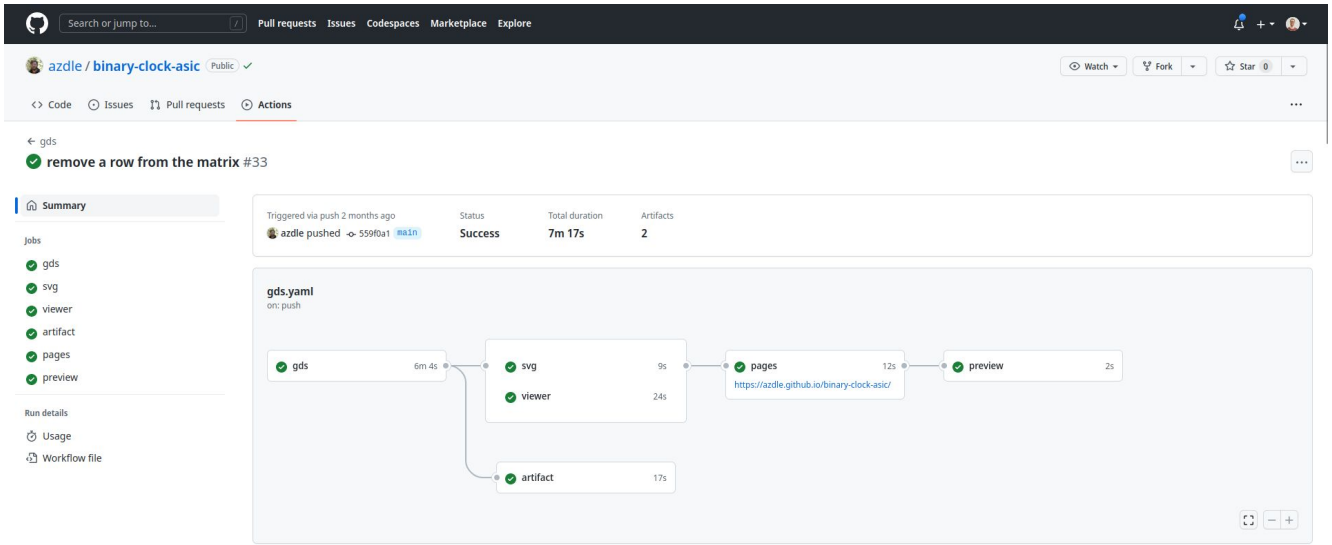
```
$ flow.tcl -design spm -tag my-spm
$ flow.tcl -design spm -tag my-spm -gui
$ ./openlane_summary/summary.py --design spm --summary
$ ./openlane_summary/summary.py --design spm --yosys-report
$ ./openlane_summary/summary.py --design spm --gds
```

Online chip development



digital-inverter-openlane.ipynb - Colaboratory

Tiny Tapeout CI



GH Actions view; GDS view

People

Yosys

2.5k stars on GitHub
A recent month in Yosys:

Excluding merges, **10 authors** have pushed **44 commits** to master and **48 commits** to all branches. On master, **80 files** have changed and there have been **6,027 additions** and **382 deletions**.

Verilator

1.5k stars on GitHub
A recent month in Verilator:

Excluding merges, **20 authors** have pushed **94 commits** to master and **96 commits** to all branches. On master, **534 files** have changed and there have been **7,073 additions** and **2,375 deletions**.

cocotb

1.3k stars on GitHub

A recent month in cocotb:

> Excluding merges, **7 authors** have pushed **11 commits** to master and **12 commits** to all branches. On master, **23 files** have changed and there have been **295 additions** and **23 deletions**.

Skwater 130 PDK

2.5k stars on GitHub
A recent month in Skywater:

> Excluding merges, **1 author** has pushed **1 commit** to main and **1 commit** to all branches. On main, **1 file** has changed and there have been **1 additions** and **1 deletions**.

OpenLane

800 stars on GitHub
A recent month in OpenLane:

> Excluding merges, **7 authors** have pushed **25 commits** to master and **25 commits** to all branches. On master, **58 files** have changed and there have been **1,101 additions** and **1,384 deletions**.

OpenROAD

725 stars on GitHub
A recent month in OpenROAD:

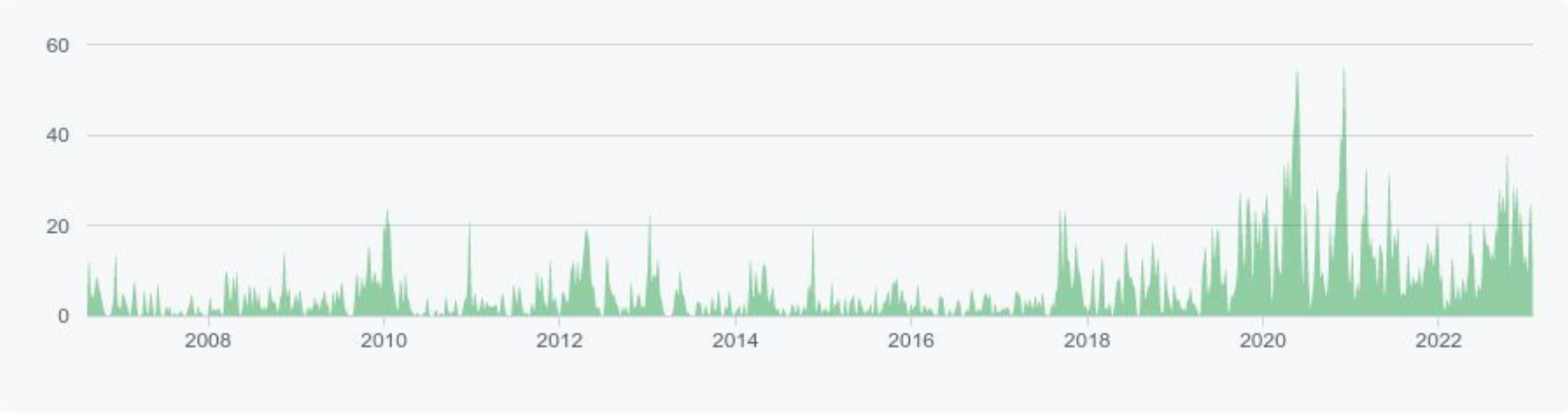
> Excluding merges, **19 authors** have pushed **325 commits** to master and **325 commits** to all branches. On master, **583 files** have changed and there have been **46,241 additions** and **390,554 deletions**.

Linux

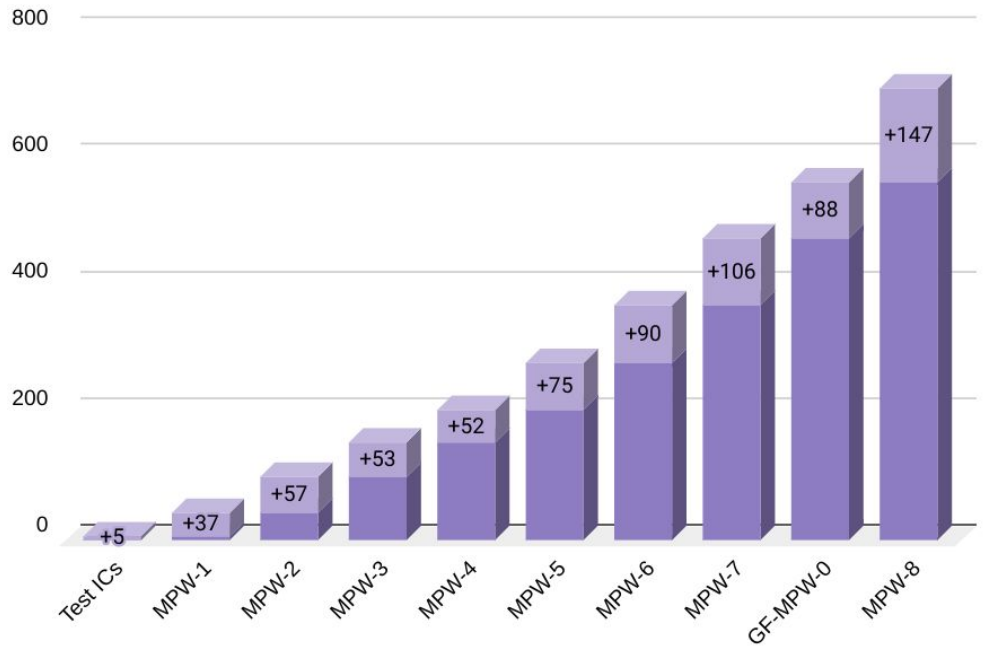
A recent month in the Linux Kernel:

Excluding merges, **505 authors** have pushed **1,021 commits** to master and **1,021 commits** to all branches. On master, **1,430 files** have changed and there have been **18,570 additions** and **9,814 deletions**.

Verilator, a growing community



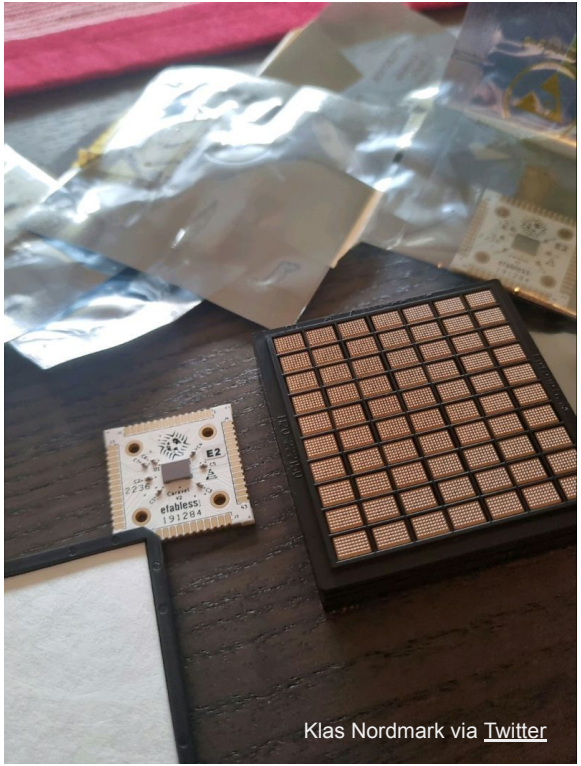
More chip designs!



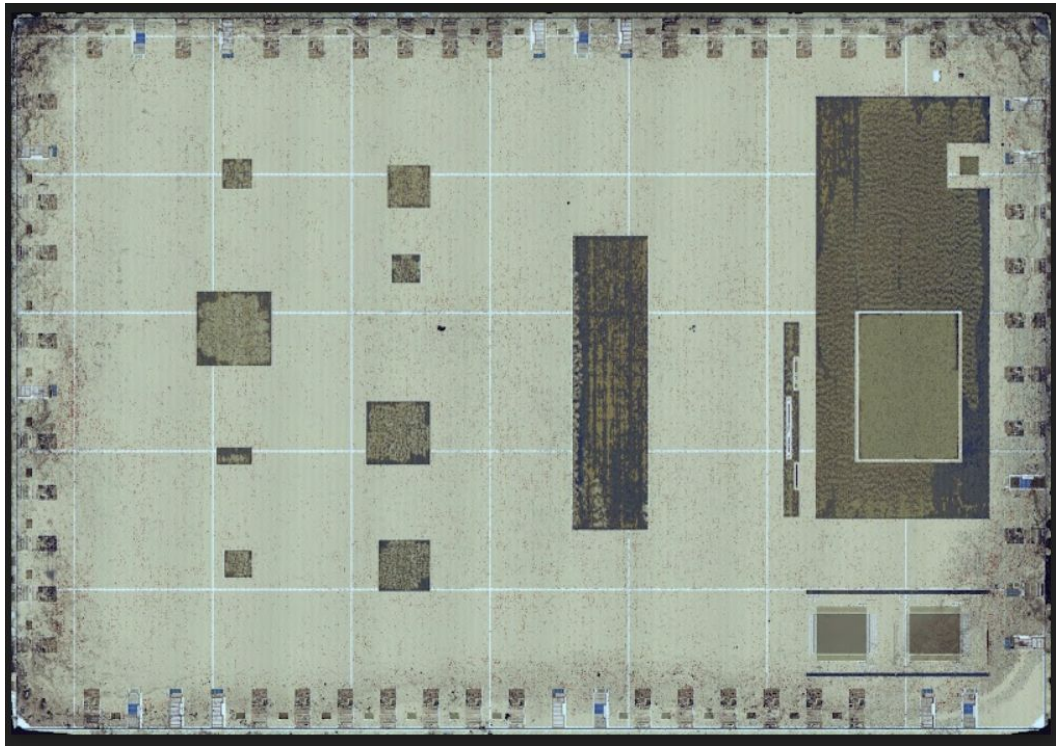
Number of chip designs **submitted** to OpenMPW – not all of them are being manufactured!

The FOSSi Foundation.

Chips are back!



Klas Nordmark via Twitter


Bare die photo by Olivier at explained via Matt Venn.

The Future

What does the future hold?

- Unpredictable innovation.
- Simpler, more accessible, better tools.
- Democratized access! (part of it: cost)
- Revolutionize learning!

Learn more

- El Correo Libre, the monthly FOSSi Foundation newsletter. https://www.fossi-foundation.org/ecl
- Join the open-source-silicon.dev Slack with all your questions
- Give it a try: Submit to OpenMPW!
- Learn, literally! Take the Zero to ASIC Course or do a Tiny Tapeout (thanks Matt!)

In-person events are back!

ChrisGoldNY CC BY 3.0

Latch-Up 2023

Friday, March 31 to
Sunday, April 2, 2023
Santa Barbara, CA, USA

https://latchup.io

In-person events are back!

Hochschule München, CC BY-SA 4.0, via Wikimedia Commons

ORConf 2023

September 15 - 16, 2023
Munich, Germany
https://orconf.org/

An atmosphere of excitement and anticipation pervades this field. Workers from many backgrounds, computer scientists, electrical engineers, and physicists, are collaborating on a common problem area which has not yet become classical. The territory is vast, and largely unexplored. The rewards are great for those who simply press forward.

C. Mead and L. Conway, Introduction to VLSI systems. Addison-Wesley Reading, MA, 1978.

Free and Open Source Silicon is a reality today.

Join the fun!