# **CYBERUS** TECHNOLOGY

Mitigating Processor Vulnerabilities by Restructuring the Kernel Address Space

Sebastian Eydam



- Computer-Science student at BTU Cottbus since 2015
- Cyberus Technology intern since 2017
- Cyberus Technology employee since 2022



- german cyber security software company
- founded in 2017
- focus on secure virtualization and automated software testing
- https://www.cyberus-technology.de/blog.html
- https://github.com/cyberus-technology/hedron



• processor-level vulnerabilities allow attackers in userspace to leak information from kernel address space





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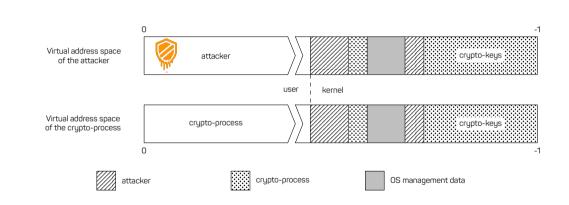
- processor-level vulnerabilities allow attackers in userspace to leak information from kernel address space
- existing mitigations introduce costly instructions into performance critical parts of the kernel
- investigate an alternative mitigation strategy on the kernel design level that ideally adds no runtime overhead and is CPU independent



**Talking Points** 

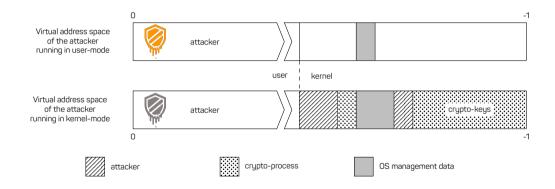


**Current Status Proposed Mitigation Case-Study: Hedron Measurement** Efficacy Conclusion



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• Kernel Page-Table Isolation: 5% - 30%



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- Speculative Load Hardening: 10% 50%



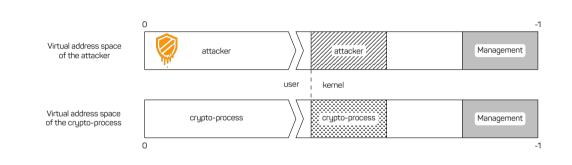
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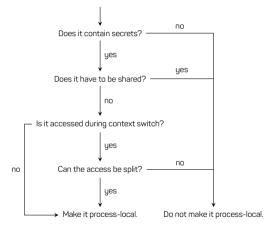
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- Indirect Branch Control: 20% 50%



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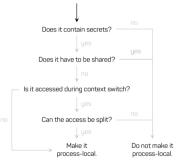


# UTCB

Does it contain secrets?

Does it have to be shared?

Is it accessed during context switch?



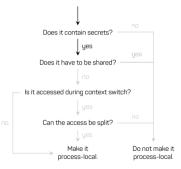


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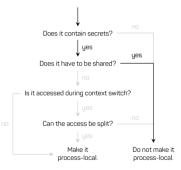


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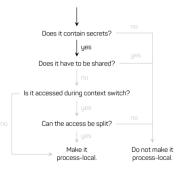




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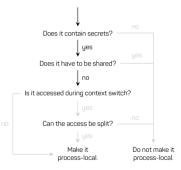




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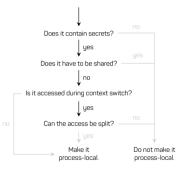




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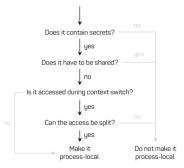




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The prototype needed ...

• a memory allocator for process-local memory



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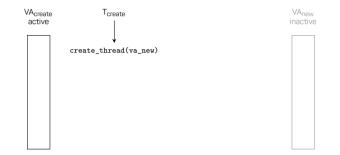
- a memory allocator for process-local memory
- slight modifications of the context switch



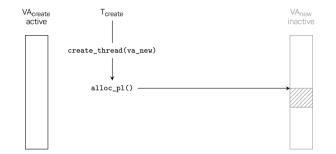
The prototype needed ...

- a memory allocator for process-local memory
- slight modifications of the context switch
- a mechanism to initialize process-local memory

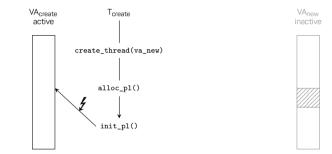














• focused on the context switch mechanism



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- microbenchmark

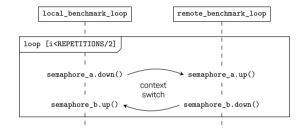


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- microbenchmark
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- Windows DiskSpd

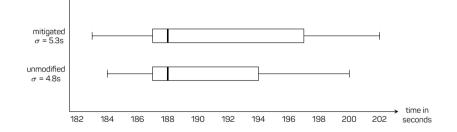


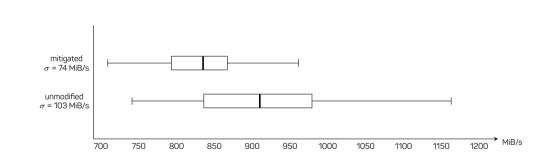




	Hedron (unmodified)	Hedron with mitigation
Cycles per context switch	2294	2315

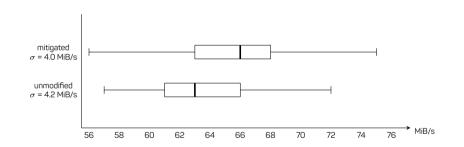






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Mitigation	Meltdown	Spectre v1	Spectre v2	илкпоwn	<sup>zero</sup> cost	CPU independent
Kernel Page Table Isolation						
Disabling speculative execution						
Speculative Load Hardening						
Retpolines						
Indirect Branch Control						
Proposed Mitigation						



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- https://github.com/amphi/hedron/tree/new-mitigation-prototype