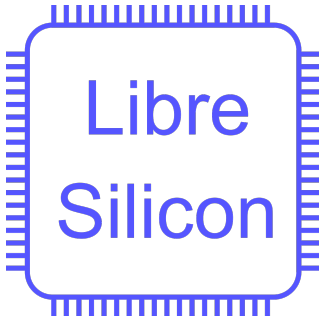


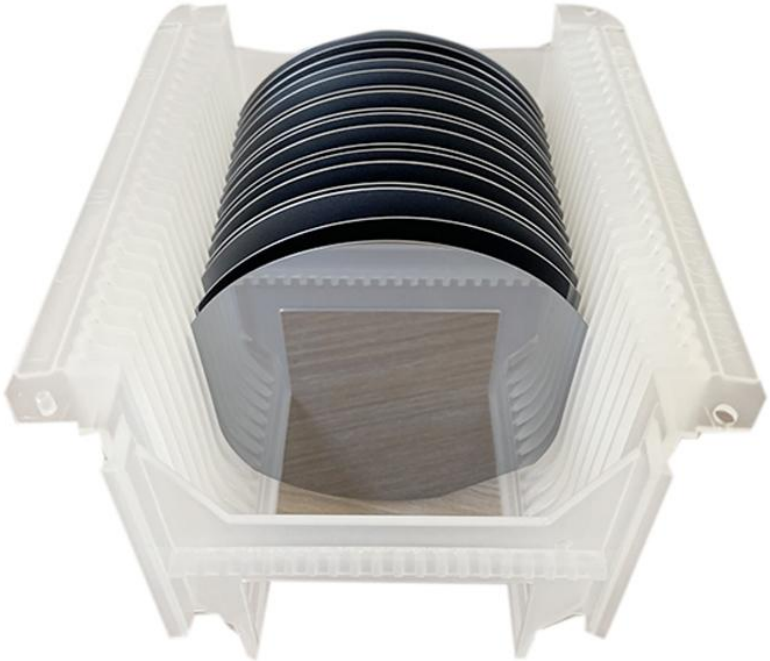
Using LibreSilicon

The Leviathan

January 19, 2022

How to actually use the process and scale it

Batch loading



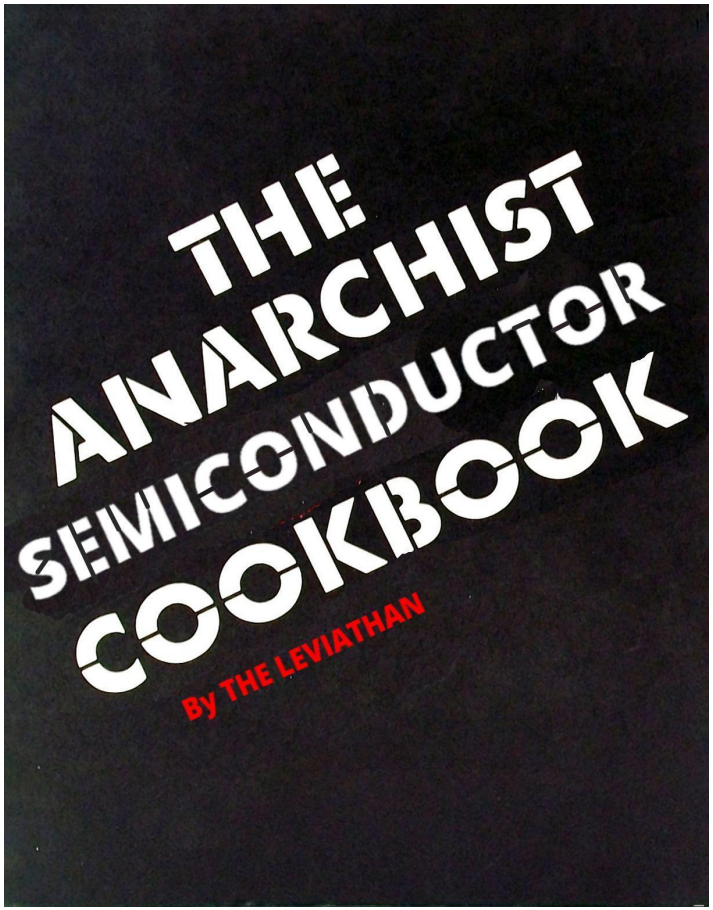
Manual loading

Reasons for LibreSilicon

- Vendor lock-out
- Vendor lock-in
- Supply chain shortage
- Transparency issue
- NDAs hinder cooperation and exchange of ideas
- Intellectual property laws are weaponized by countries to hurt other countries and their economy

Goal of LibreSilicon

- A scalable open platform
- Generalized open process flow
- Collection of chemical recipes
- Brief overview over diverse machines

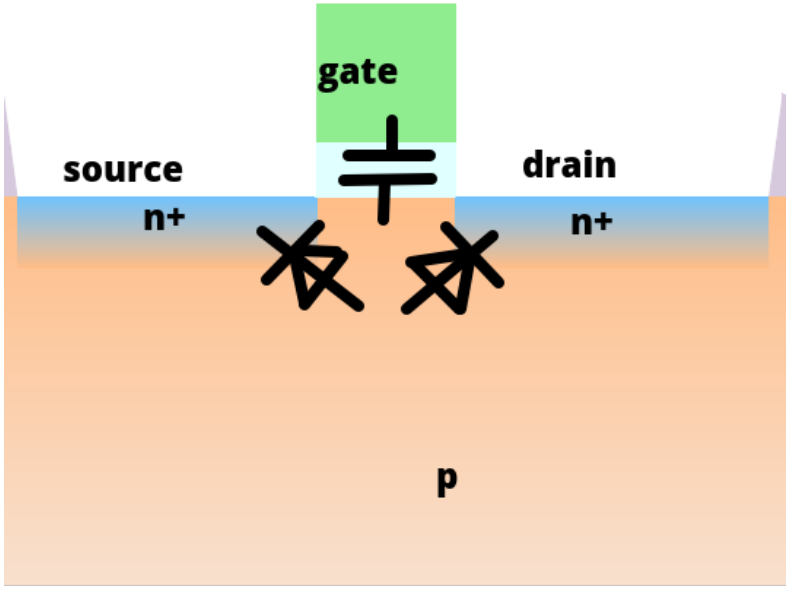


Goal of LibreSilicon

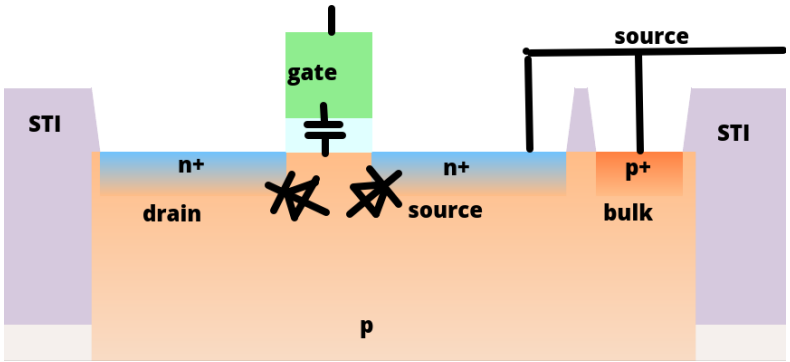
I came, I saw, I made some micro structures:

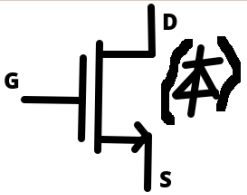
Theoretical CMOS

nMOS



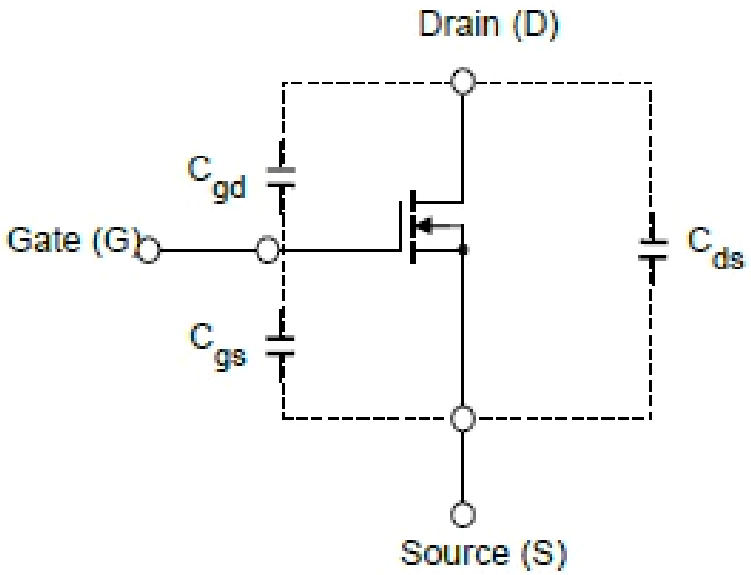
nFET

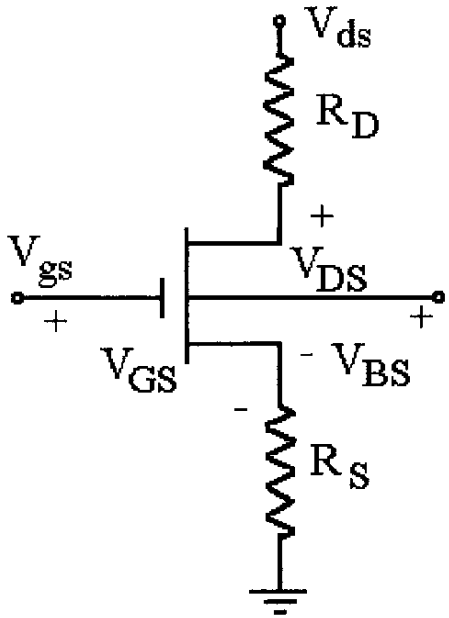




Physical properties

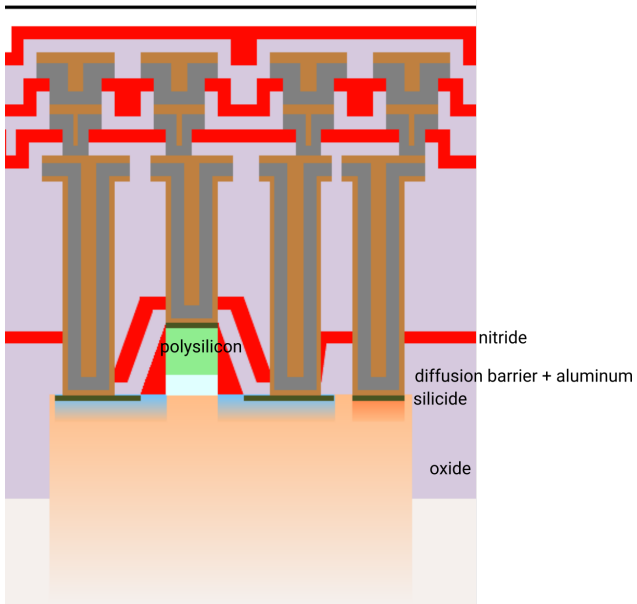
- Capacities
  - Oxide between interconnects (worsened due to high-κ material)
  - Space between bonding wires
  - Gate oxide thickness
  - etc.
- Resistance
  - Contacts: Bonding, interconnect, etc.
  - Channel resistance
  - etc.





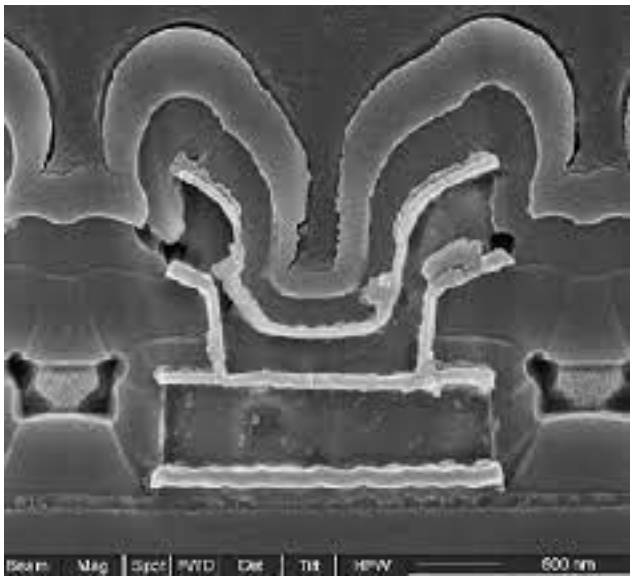
Cruel reality CMOS

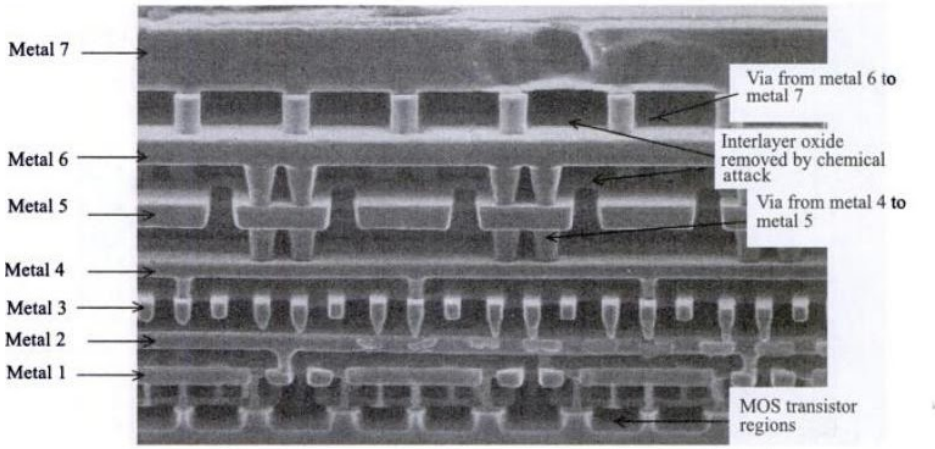
- Many nitride (high-κ) layers for CMP (polishing) endstops
- Silicide in order to reduce sheet resistance
- Nickel on top of silicide as diffusion barrier to Aluminum
- Trench/LOCOS isolation



Planarization: CMP

Without planarizing between the metal steps, multilayer interconnects are impractical: planarization is a **must have**



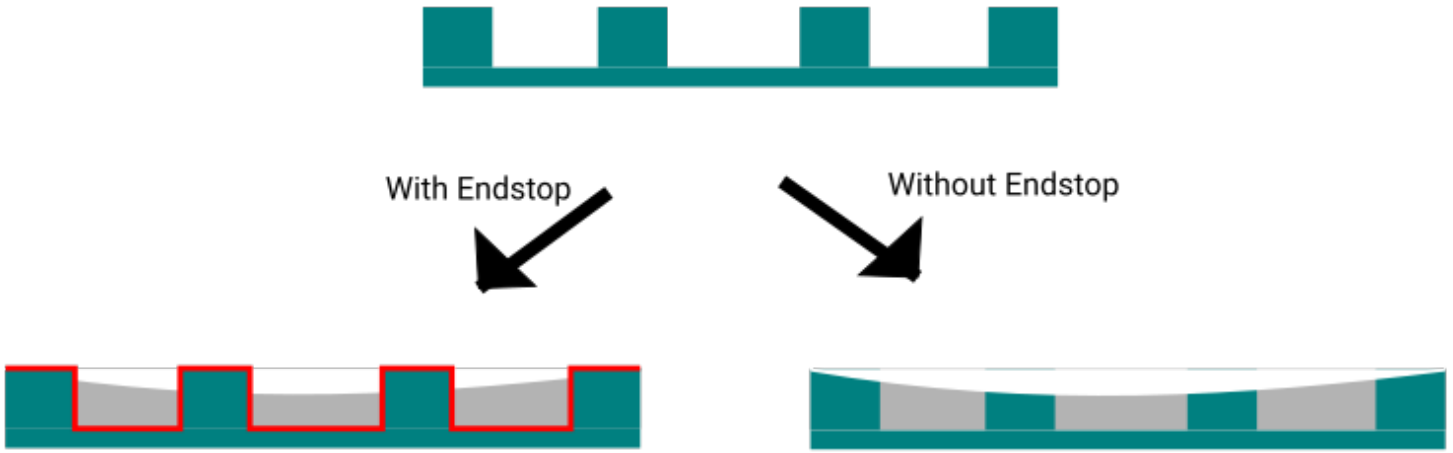


Cross-section of a 0.12 µm technology (*Courtesy:* Fujitsu)

Planarization: CMP

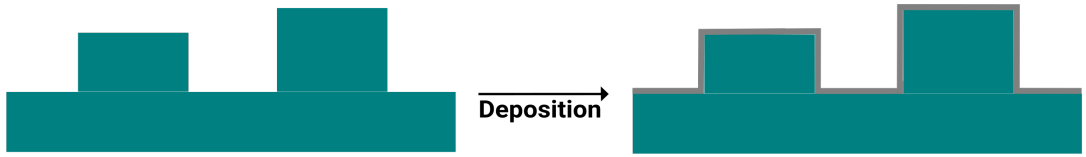
Without endstop we would

- Destroy interconnect wires
- Cause crystal damage

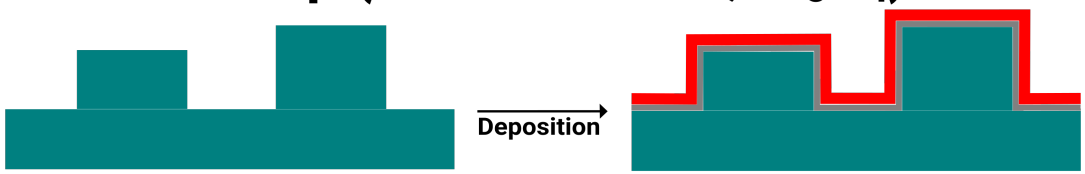


Planarization: CMP

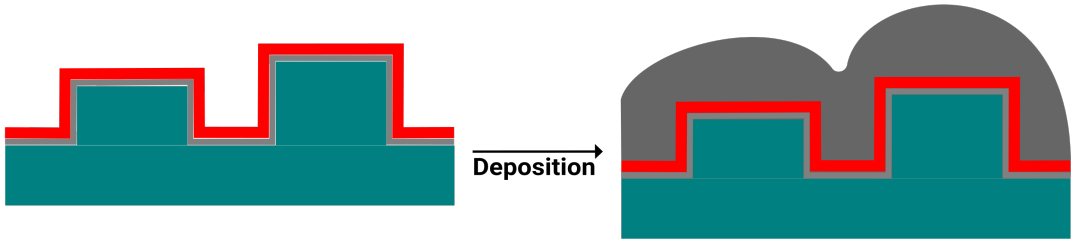
Pad-oxide (LTO, Low Temperature Oxide, SiO_2)



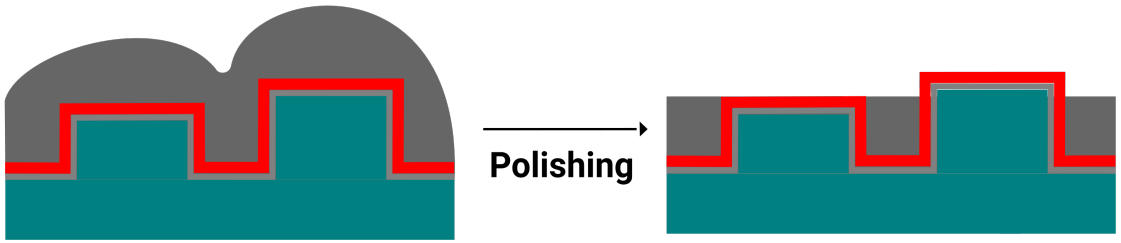
End-stop (Silicon nitride, Si_3N_4)



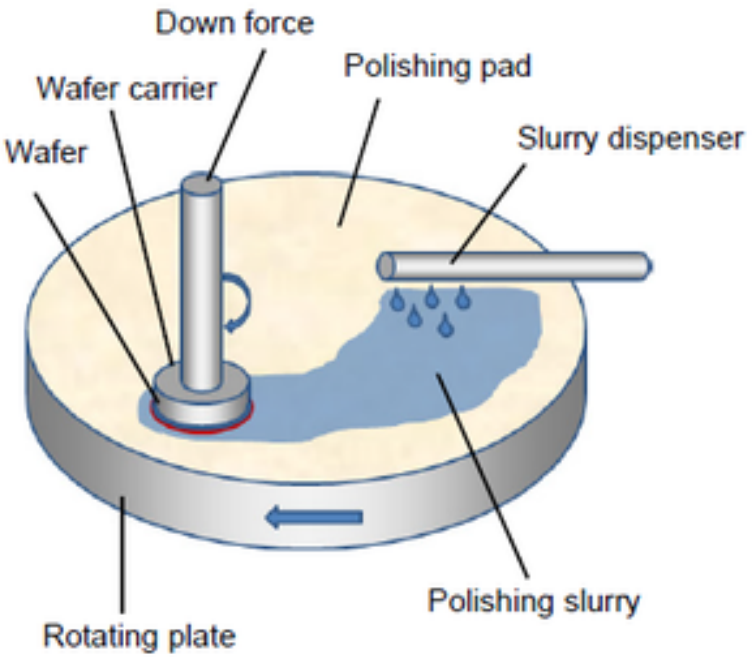
Isolation (LTO, Low Temperature Oxide, SiO_2)



CMP (Chemical Mechanical Planarization)



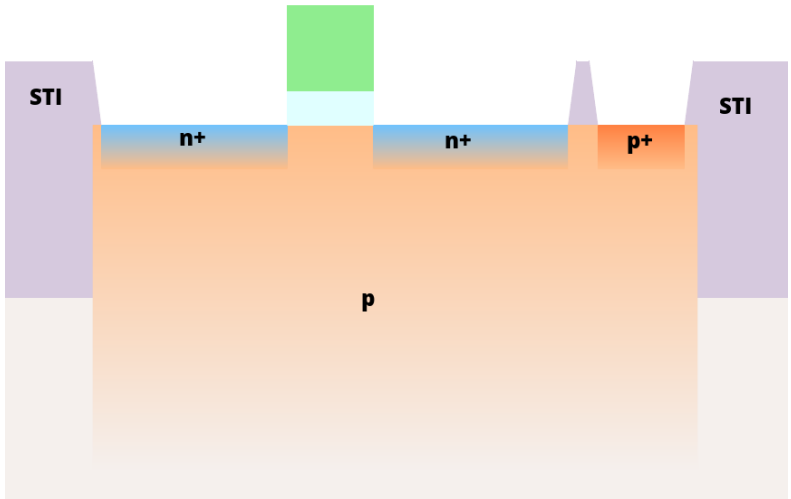
Planarization: CMP



6000-ish USD

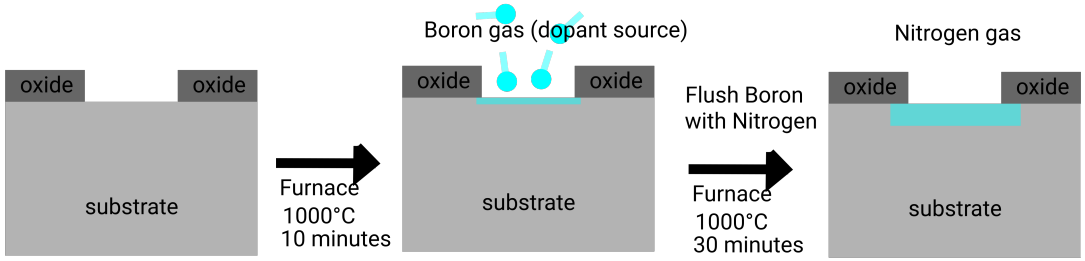
Putting stuff into the silicon (Doping)

- Silicon is a **semi**conductor
- Either n (more electrons) or p (more "holes") doping:
  - n: Usually Phosphorus
  - p: Usually Boron
- Doping material source either gas/liquid

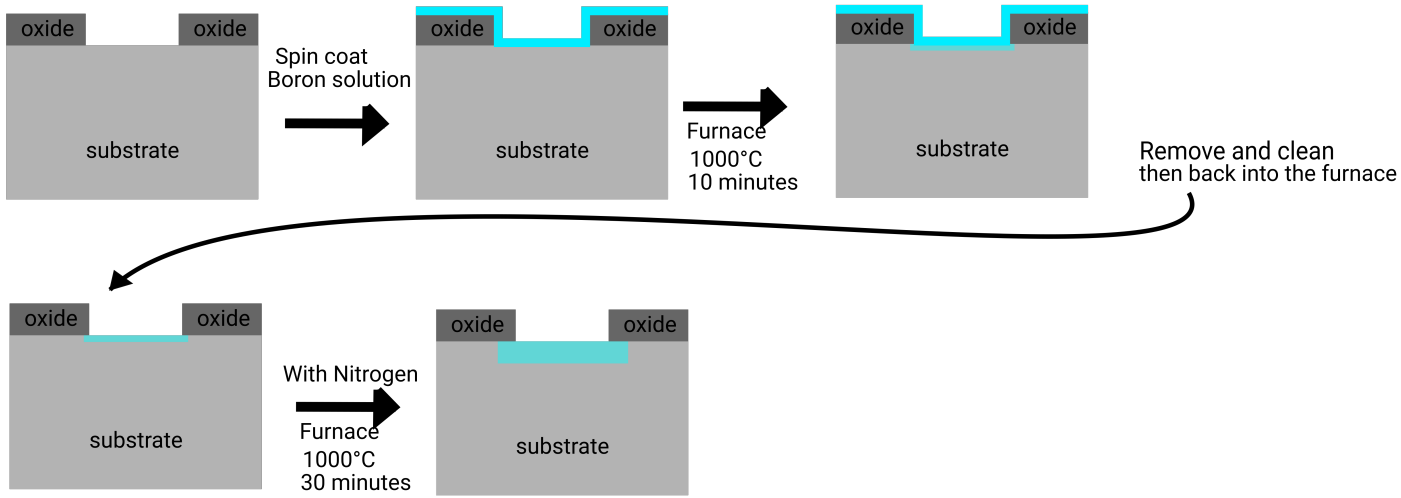


Doping: Diffusion

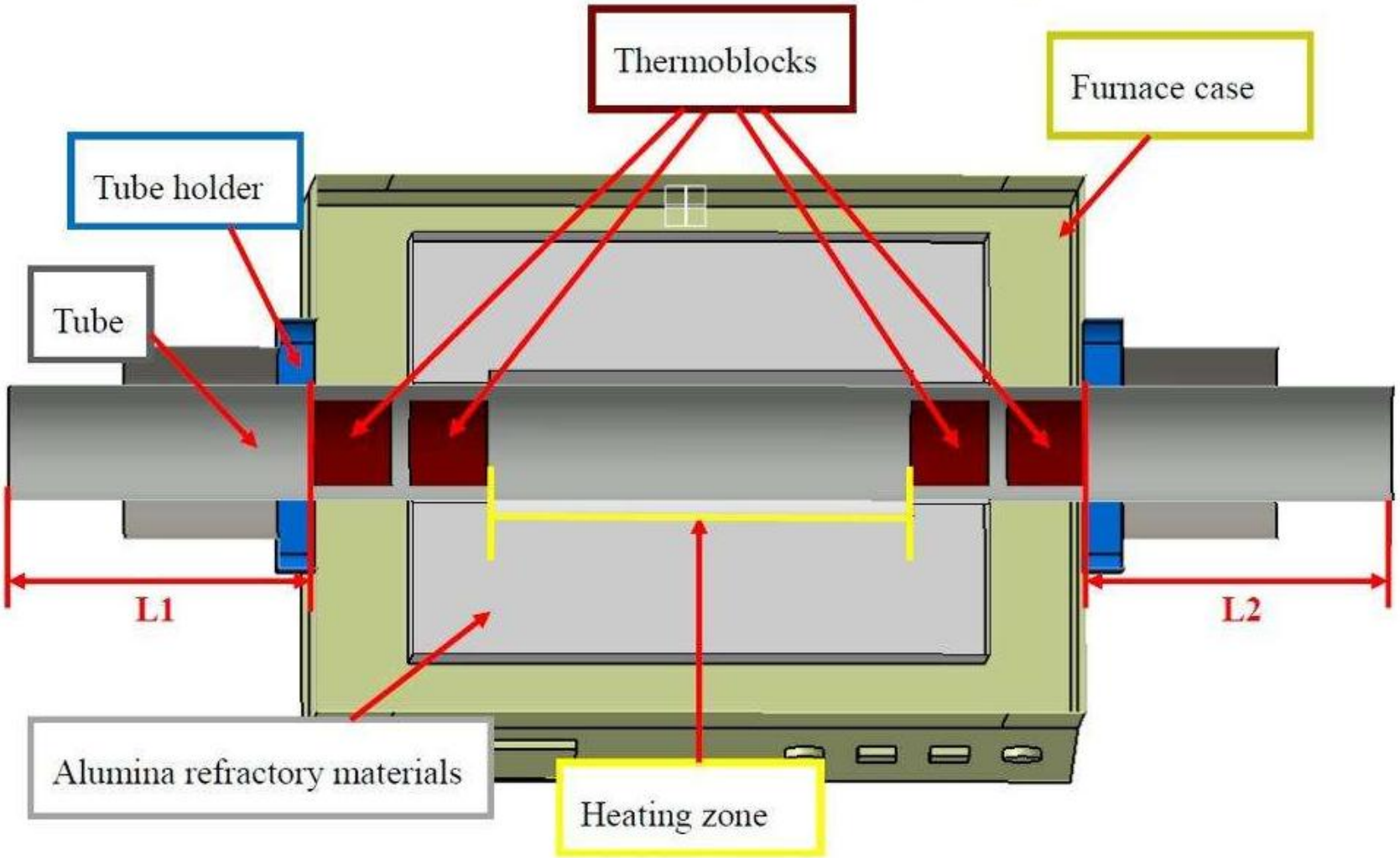
Gas predeposition



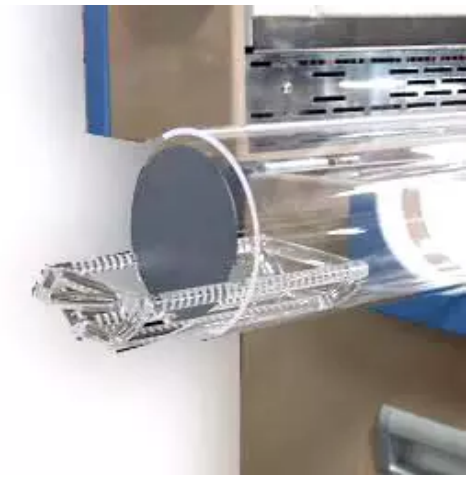
Liquid predeposition



Tube furnace



Doping: Diffusion



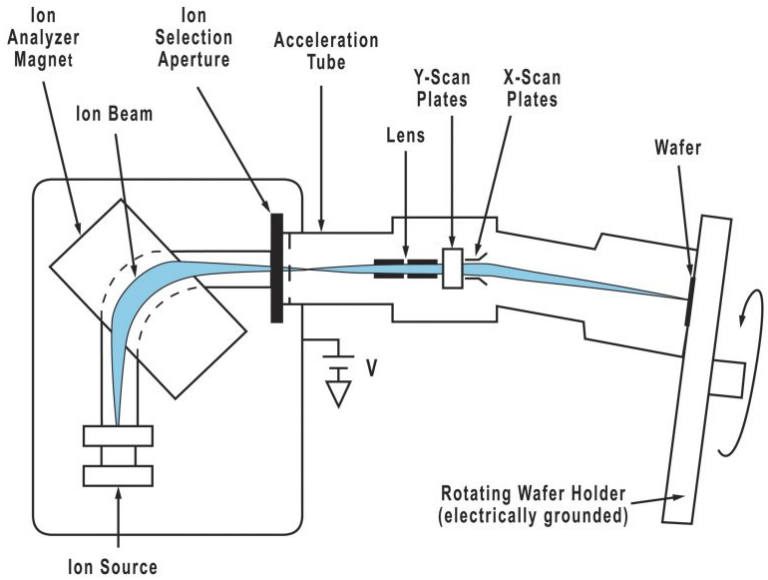
Doping: Diffusion

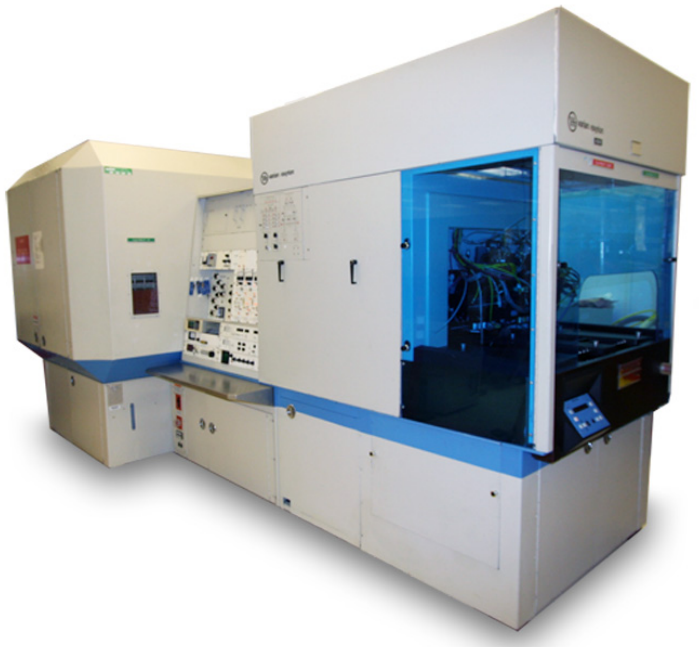
(Industrial scale)

This one is up to **5000 USD**

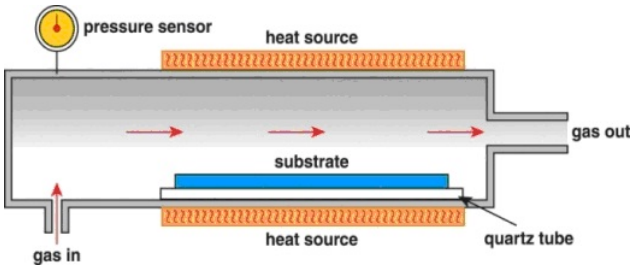
Doping: Implantation

- Same category as the giant tube furnace
- A particle accelerator shooting dopants at the wafer



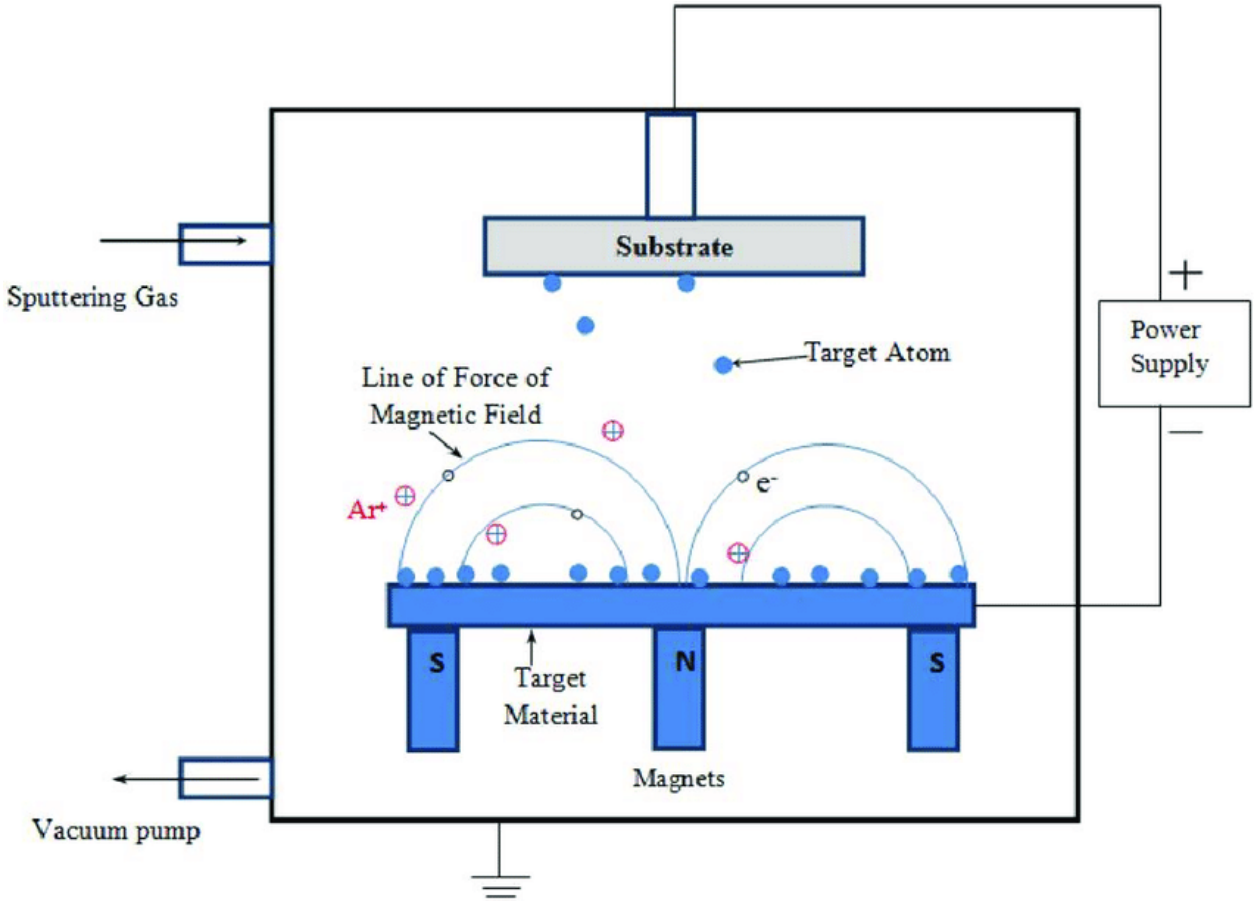


Depositing stuff: Chemical Vapor Deposition (CVD)

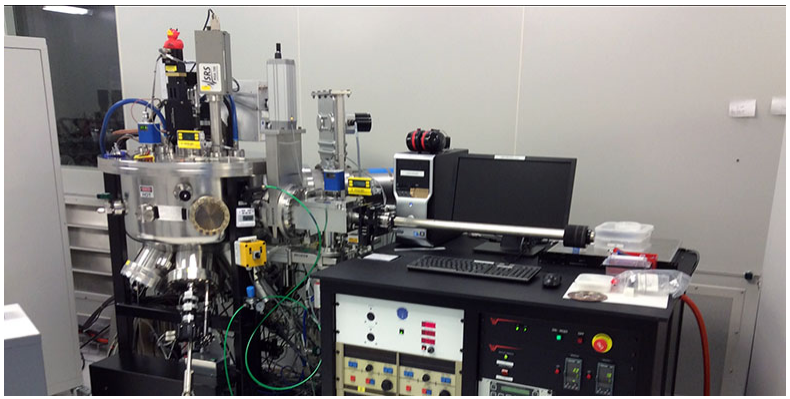


- Can be used to deposit
  - Low Temperature Oxide
  - Polysilicon (With Silane(SiH_4) gas)
  - Silicon Nitride
  - Even metals like Tungsten (with WF_6) and Aluminum (with $(Al(CH_2CH(CH_3)_2)_3)$
- Can be done with the doping furnace

Depositing stuff: Sputtering



Depositing stuff: Sputtering

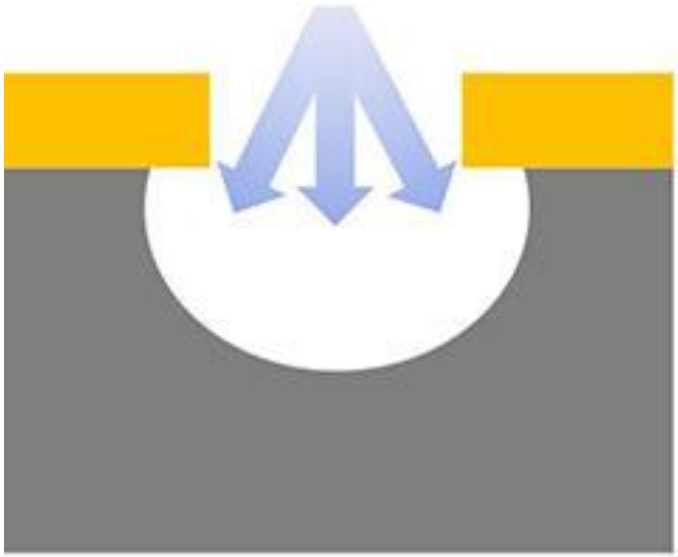


Removing stuff aka. Etching

- Wet etching, disadvantage: isotropic etching
  - Hydrofluoric acid: SiO_2, metals
  - TMAH: Silicon and polysilicon
  - KOH: Silicon and polysilicon
  - Piranha solution ($H_2SO_4 + H_2O + H_2O_2$): Cleaning unreacted metal after silicide formation
  - H_3PO_4: Nitride (Si_3N_4) @ 150°C to 180°C
- Dry etching with plasma and chemical mix, advantages
  - Anisotropics etching (Very steep angles)
  - Fine structures possibles
  - Better depth/etch rate control

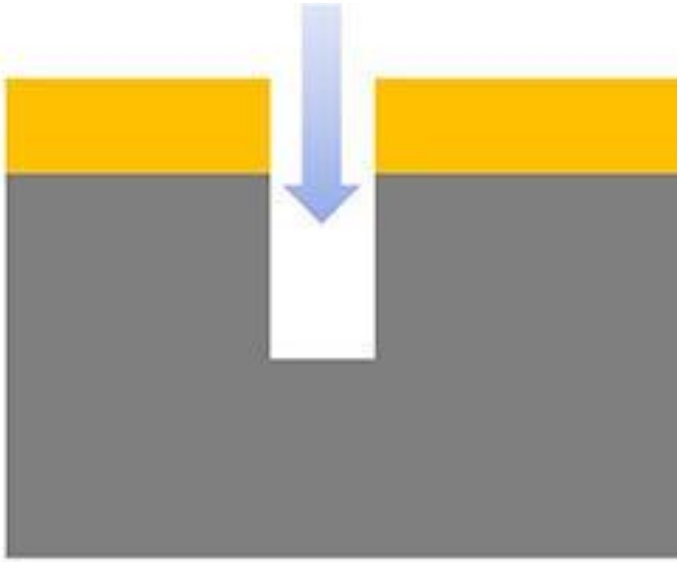
Universal: The bigger the area, the higher the etch rate!

Removing stuff aka. Etching



Isotropic Etching

Wet



Anisotropic Etching

Dry

PPE

Some of those chemicals are super duper poisonous and deadly! Herewith I told you to **wear a PPE**, so that you can't sue me in case you die.

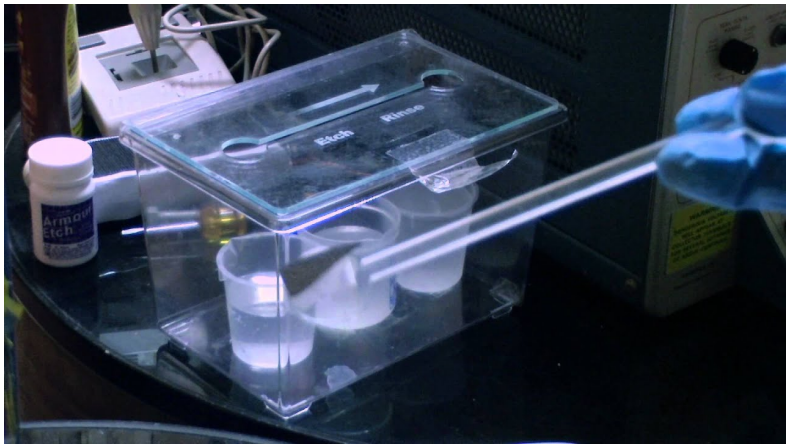
Safety goggles

Apron

Chemical resistant gloves

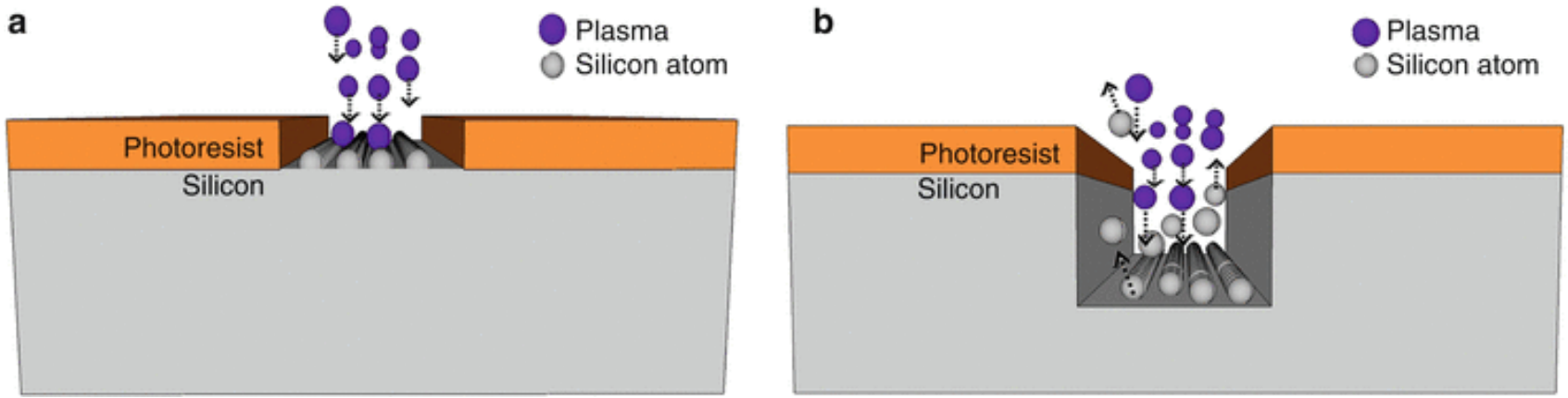
Chemical resistant face shield

Removing stuff: Wet Etching



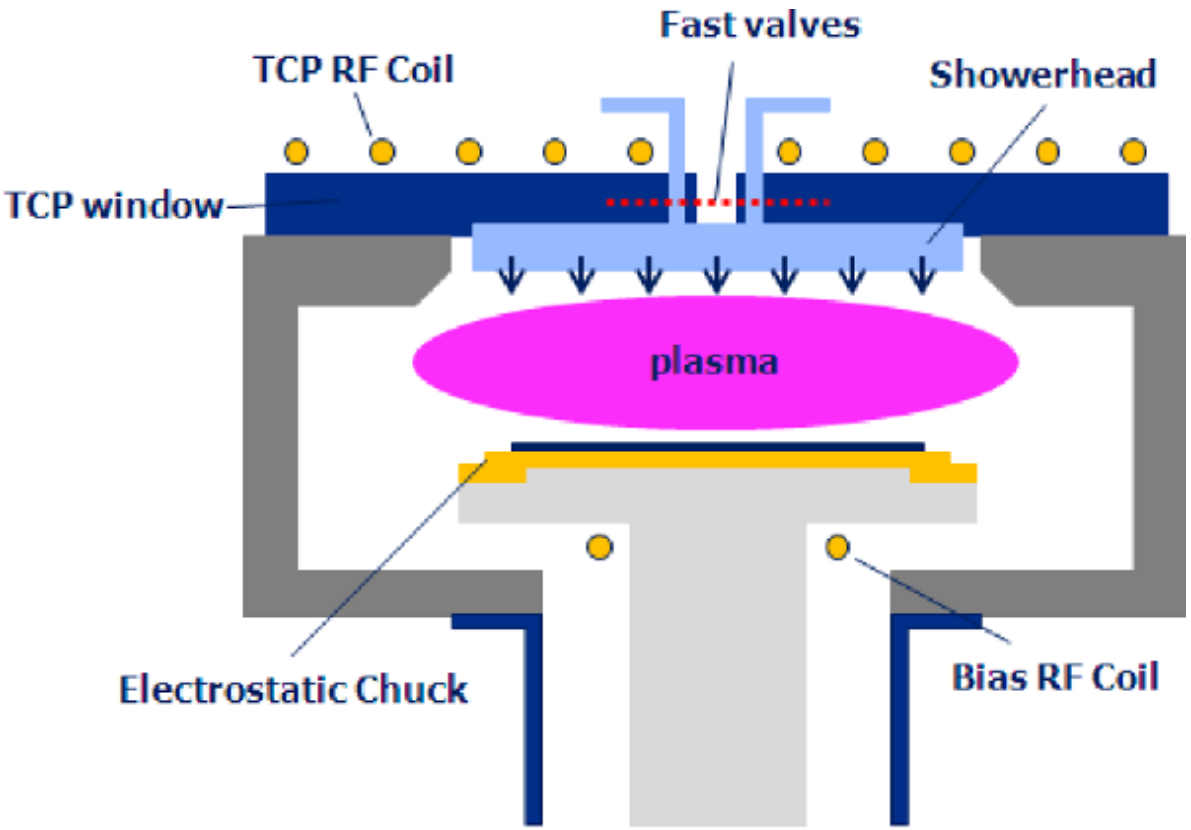
Removing stuff: Dry Etching

- "reverse sputtering"
- Argon-Chlorine and other gas mixes can be used as gas in order to improve etch rates



Removing stuff: Dry Etching

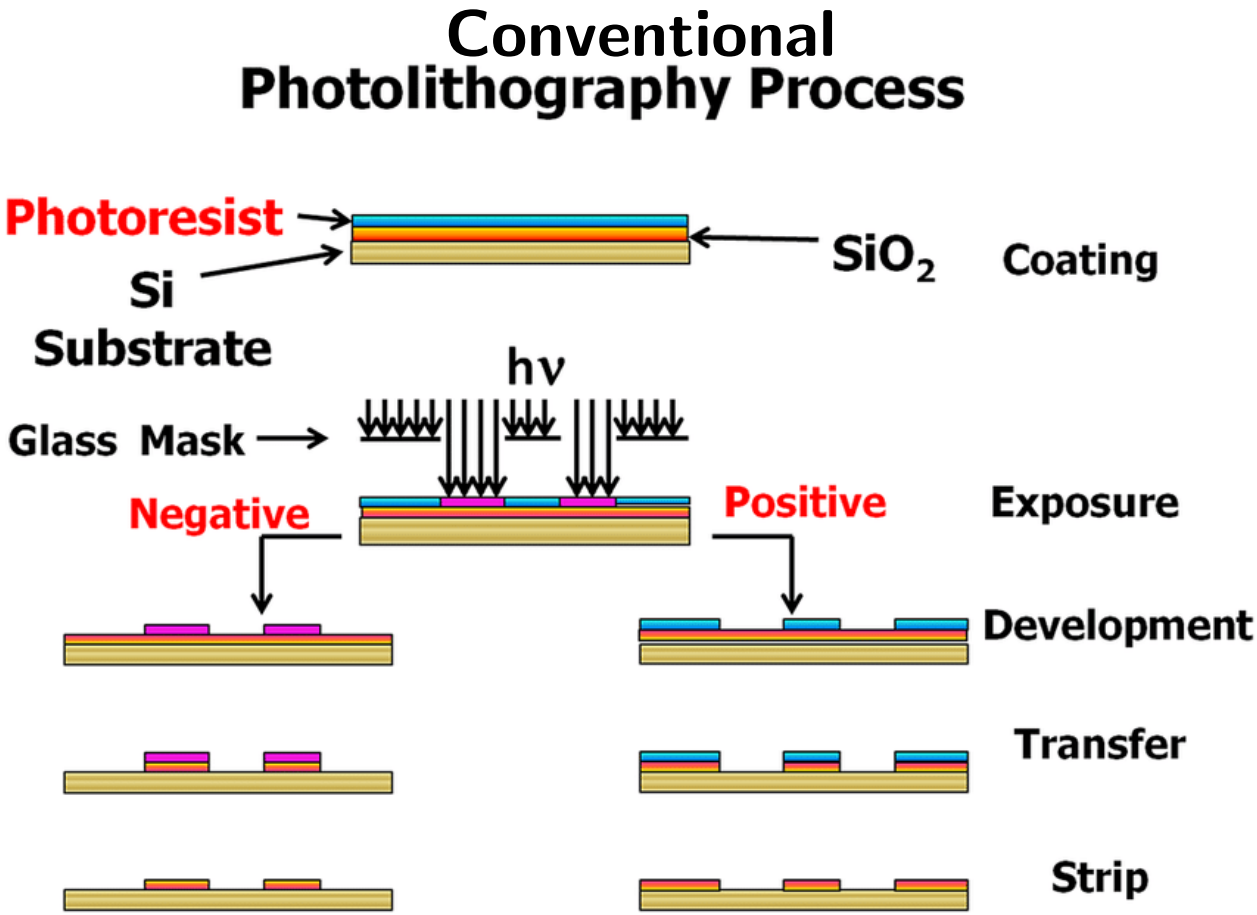
Reactive Ion Etcher



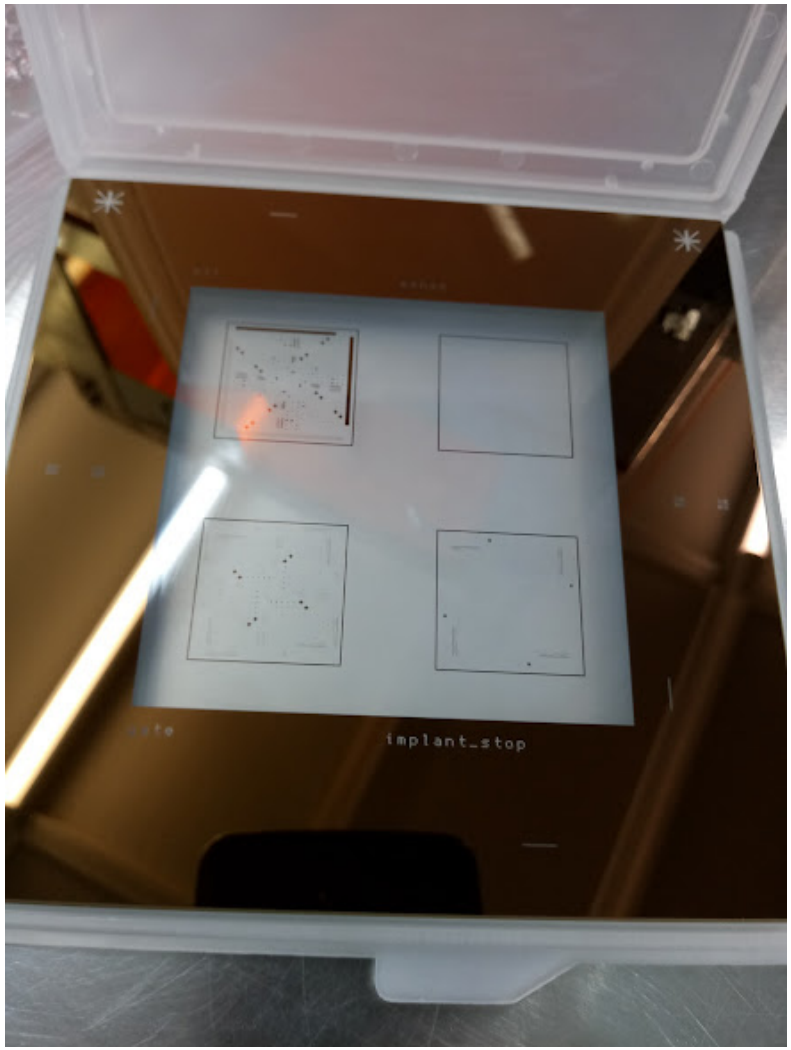
TCP: **T**ransformer **C**oupled **P**lasma

Removing stuff: Dry Etching

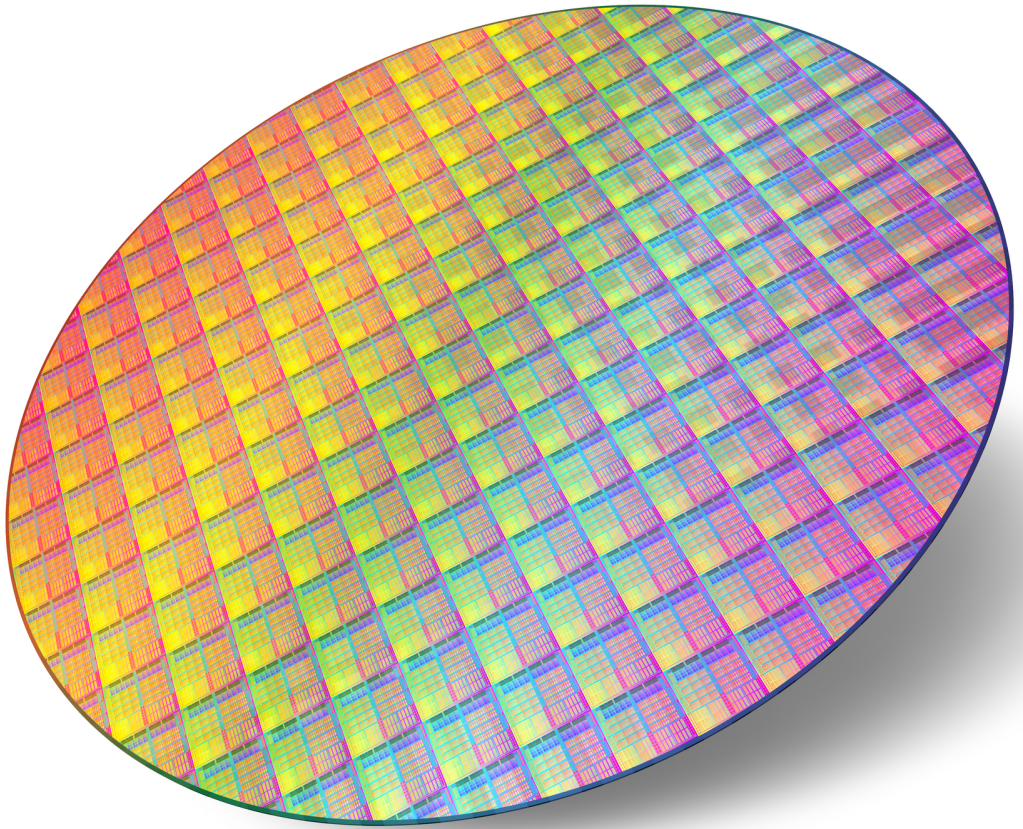
Lithography



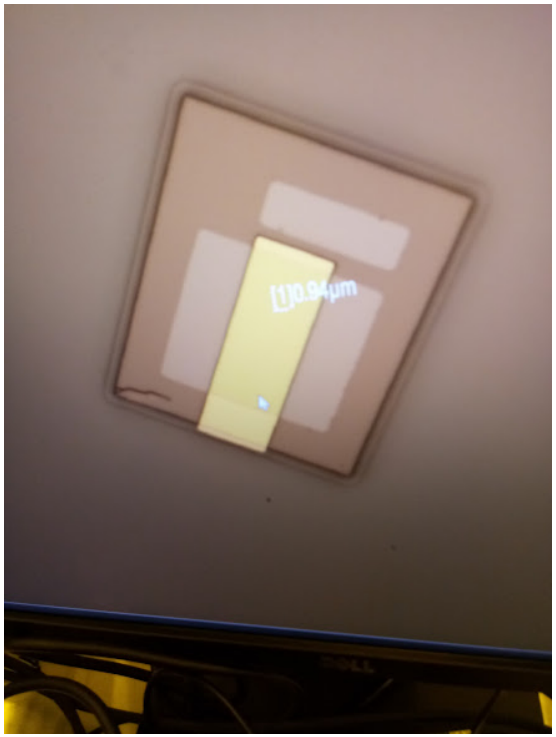
Conventional lithography

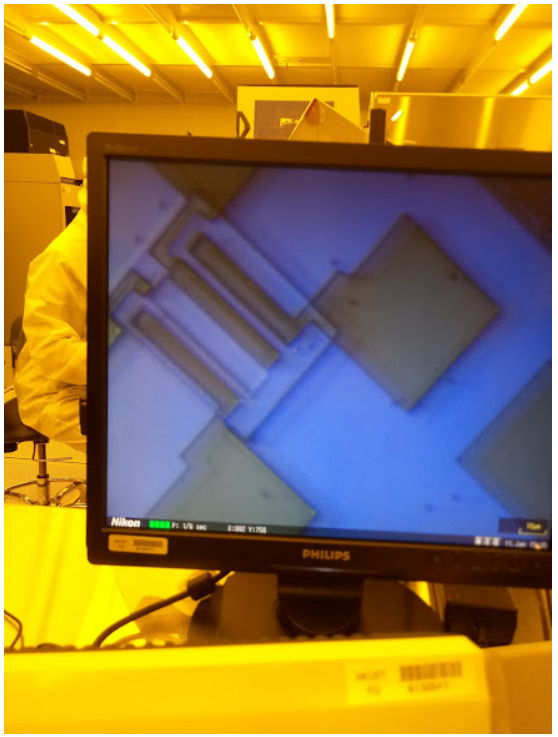


Lithography

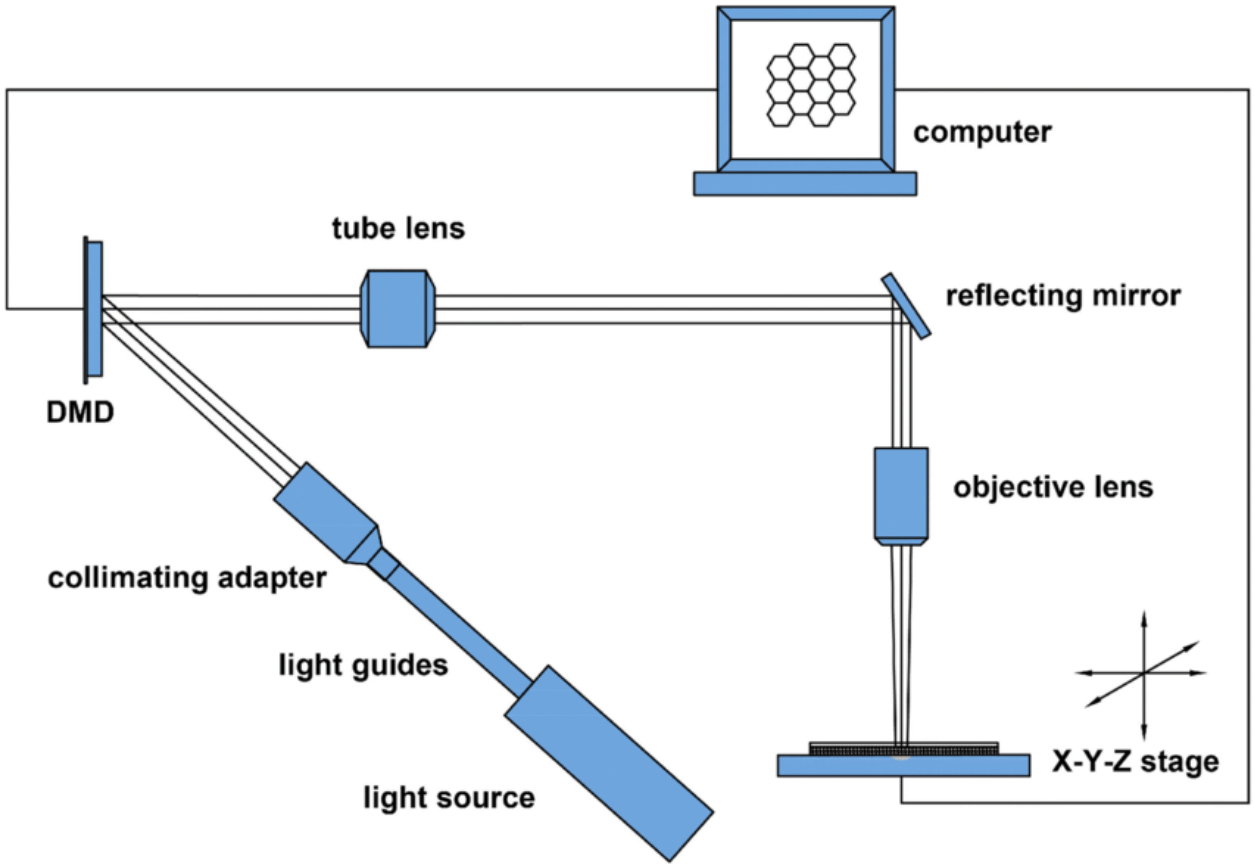


Lithography



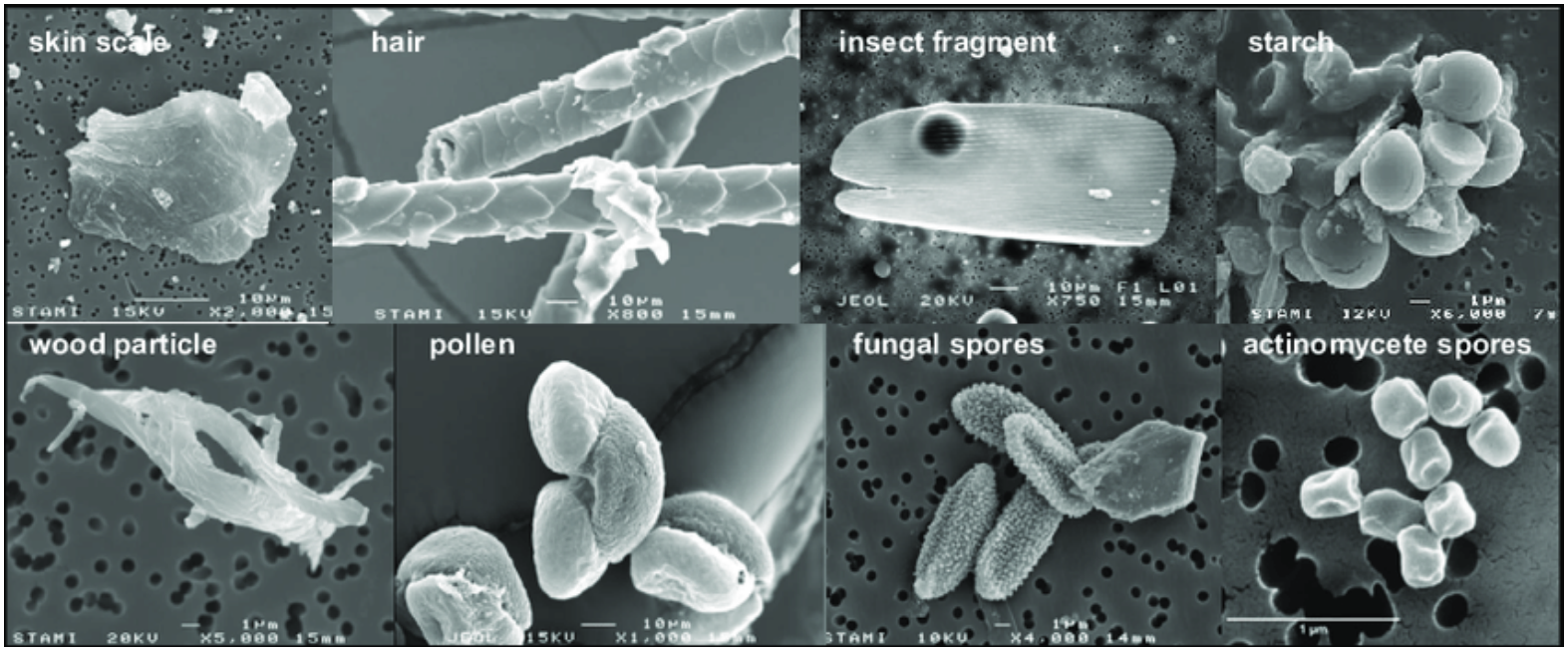


Maskless lithography

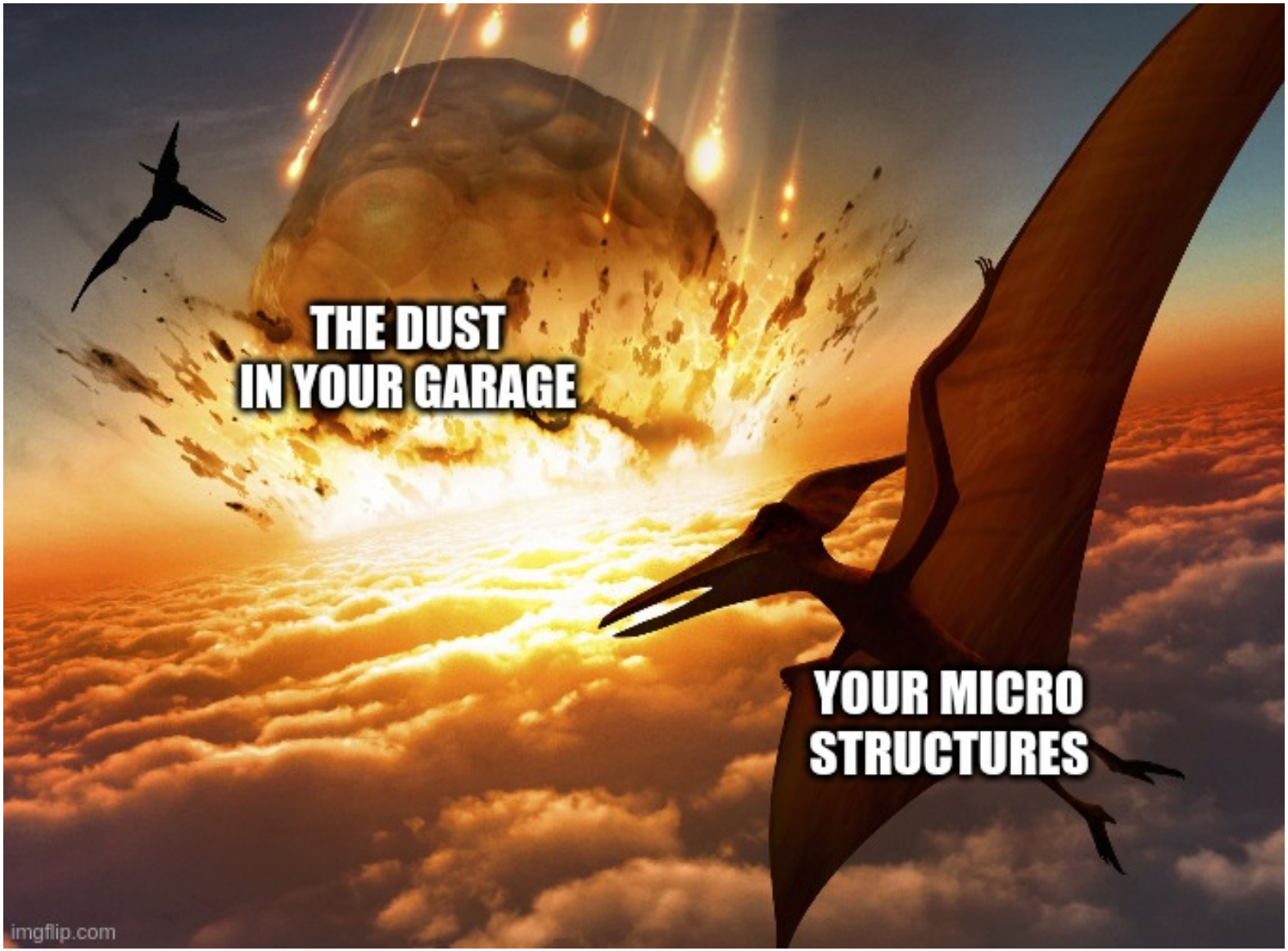


Sam Zeloof's design

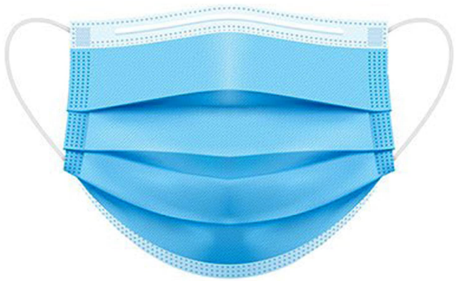
Contamination control



Contamination control



Contamination control

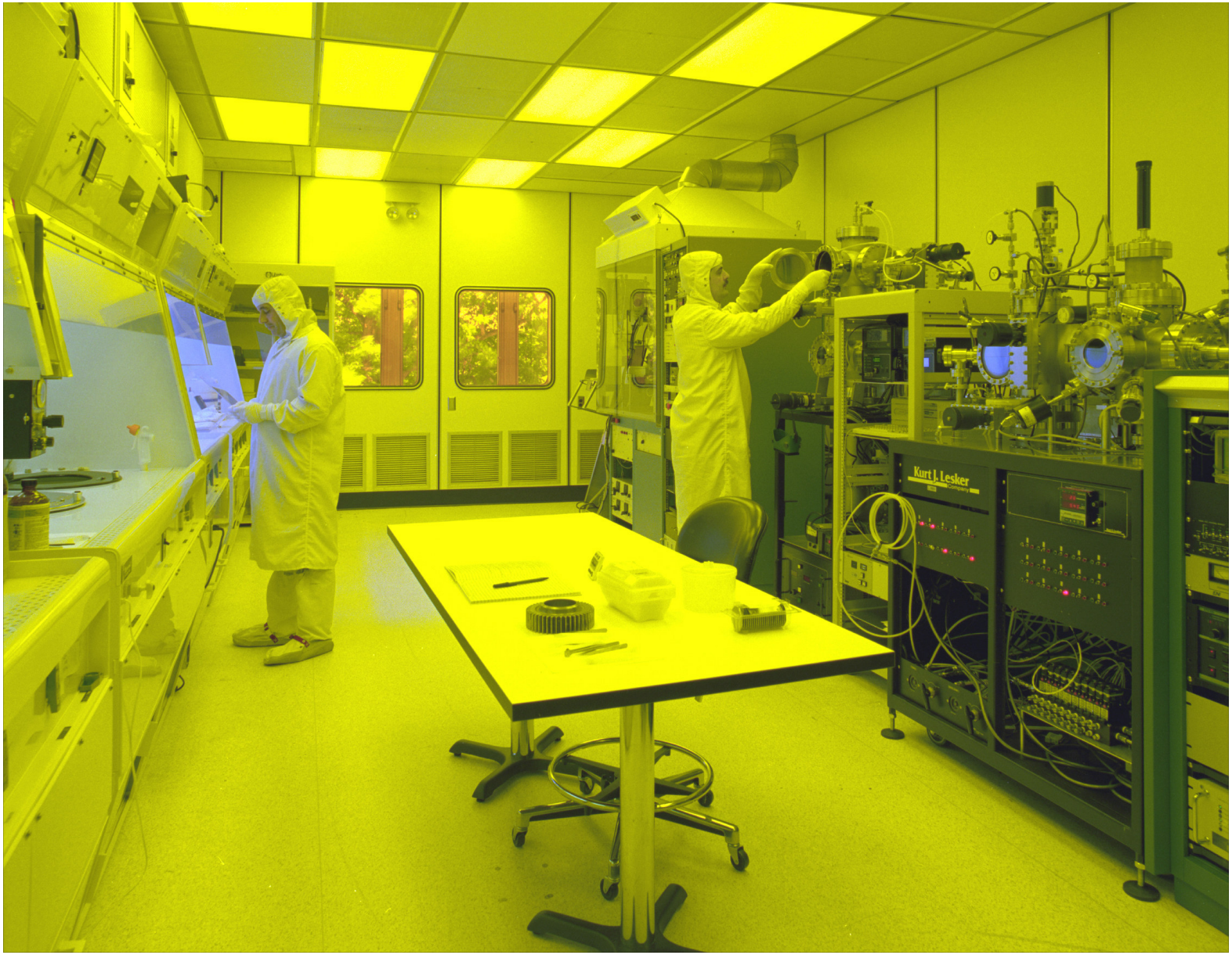


Surgical mask

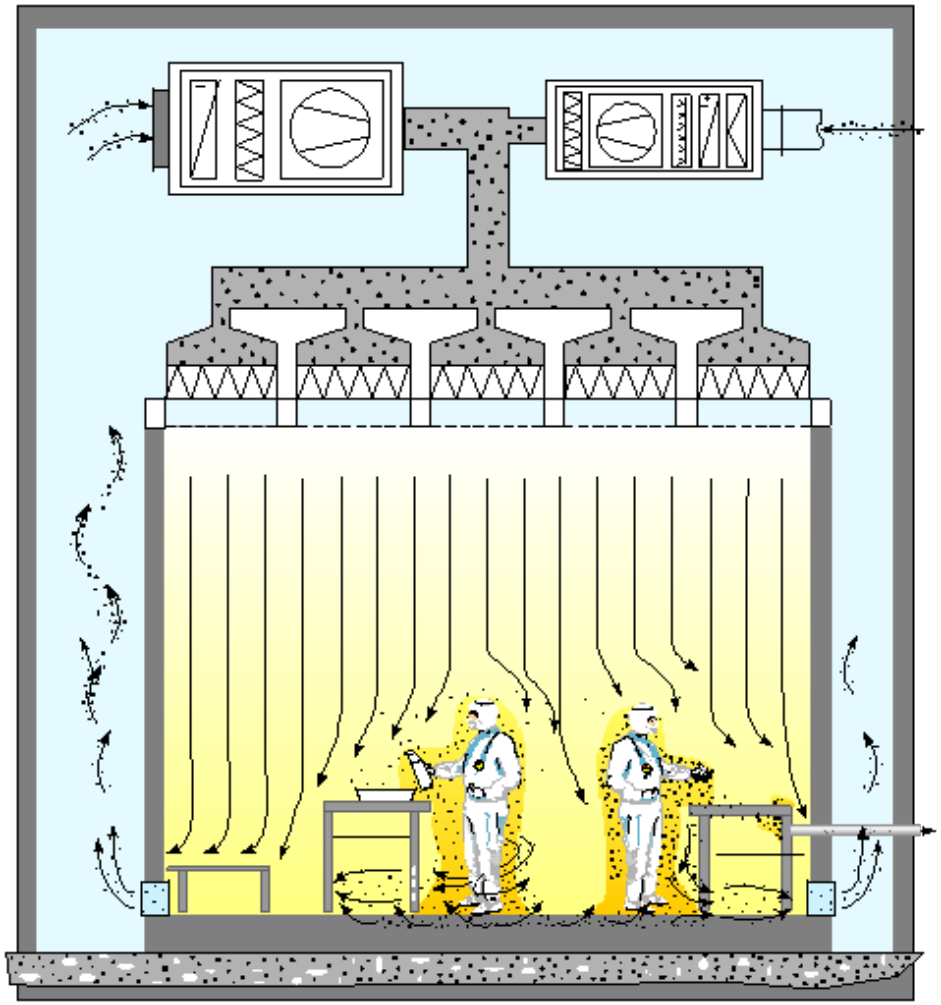
Latex gloves

Clean room garment
(Bunny suit)

Contamination control

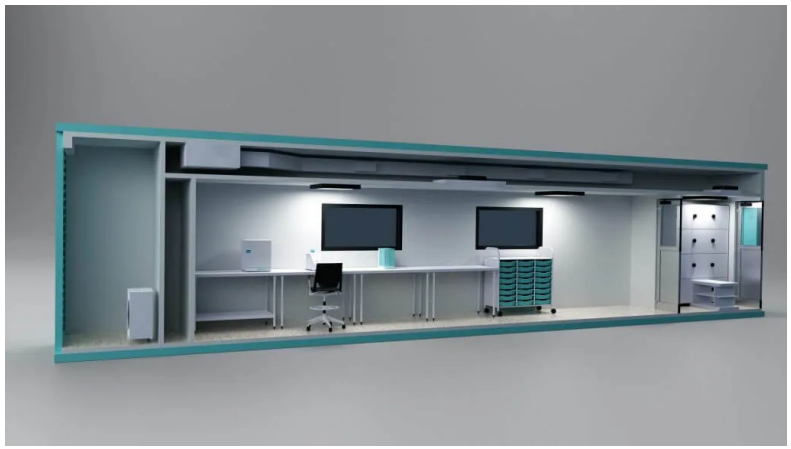


Laminar flow



Contamination control

Shipping container



Glove box

Shopping list

Must have

- CVD+Diffusion furnace
- Sputterer
- Wet station
- PPE
- Lithography system
- Microscope
- Clean room environment

Good to have

- CMP machine
- DRIE etcher

Optional

- RTP (rapid thermal processing) furnace
- Ion implanter

Process Design Kit

- Design rules due to physical constraints
  - Via size
  - Spacing
  - Area sizes
  - etc.
- Components possible to build with your setup
  - Simple stuff: Caps, Resistors, Diodes, Ls (if possible)
  - More complex stuff: ADCs, DACs, etc.
- EDA tools:
  - QFlow
  - OpenLANE
  - Magic

Check out `https://pdk.libresilicon.com`

Communication

Weekly Mumble sessions:
Every Sunday, 1800 Zulu (UTC)
Server: `murmur.libresilicon.com` (Port: 64738)

Mailing list:
`https://list.libresilicon.com/mailman/listinfo/libresilicon-developers`

Direct contact:
`leviathan@libresilicon.com`

Private donations

BitCoin (BTC):

1Ha4QrFXsjWNJLw2yhchF8bGhTKEnf9bJe

Address: 1Ha4QrFXsjWNJLw2yhchF8bGhTKEnf9bJe