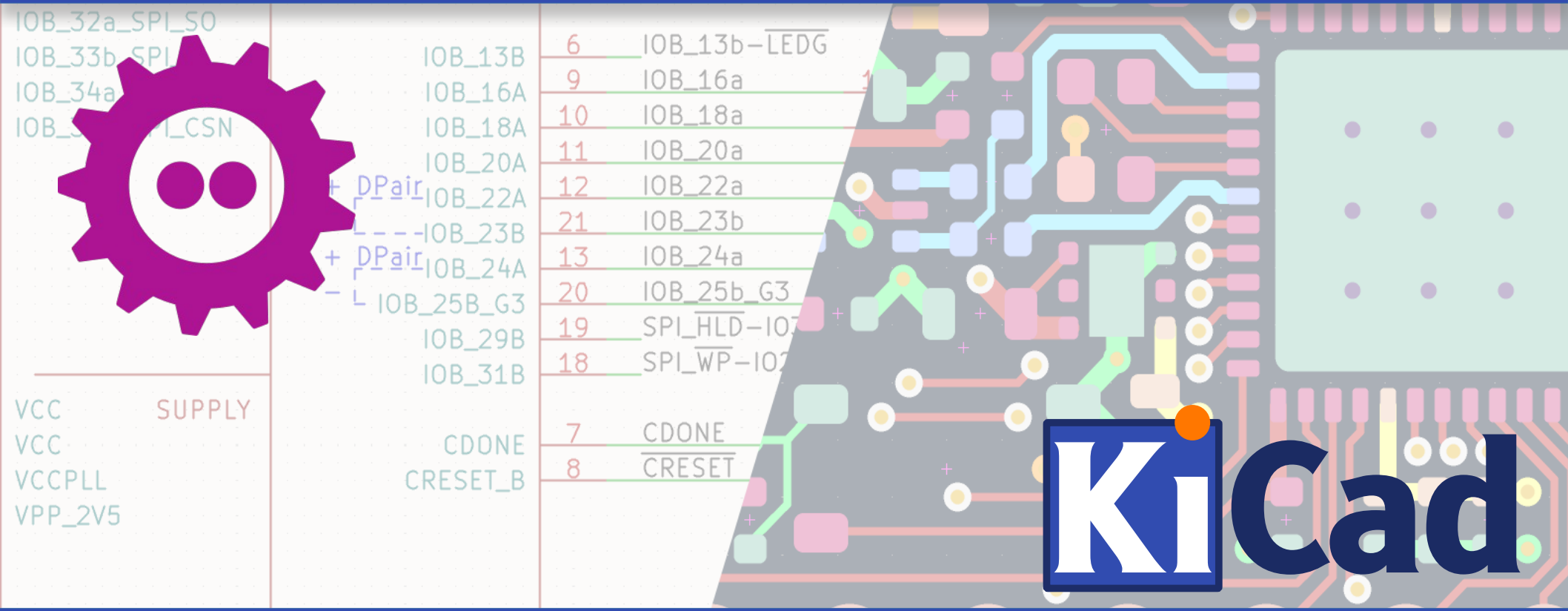
Advanced PCB simulation with KiCad

Introduction to IBIS and FEM-based simulations



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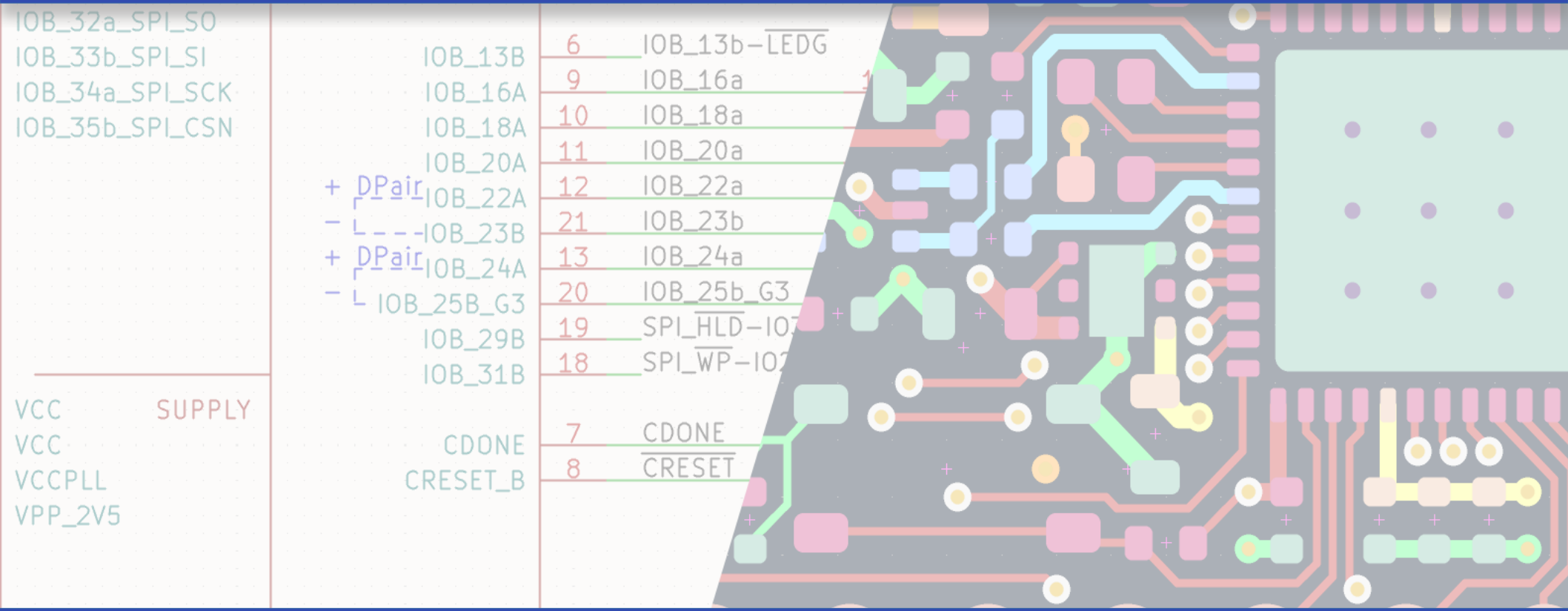
FOSDEM 2022

05/02/2022

SUMMARY

- Present state of simulation in KiCad
- FEM simulations
- Power integrity
- Signal integrity
- IBIS

Present state of simulation in KiCad

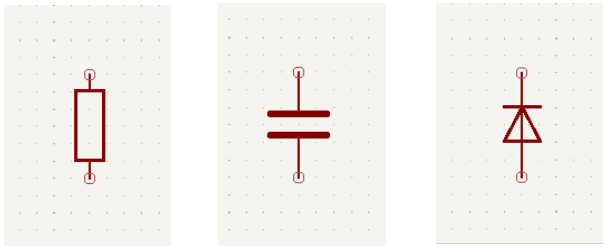


SPICE = “Simulation Program with Integrated Circuit Emphasis”

KiCad provides a graphical interface to a spice engine: ngspice.

A simulation provides a way to design and to validate a project.

$$U = RI \qquad I = C\frac{dU}{dt} \qquad I = Is\left\{e^{\frac{U}{n.V_T}} - 1\right\}$$

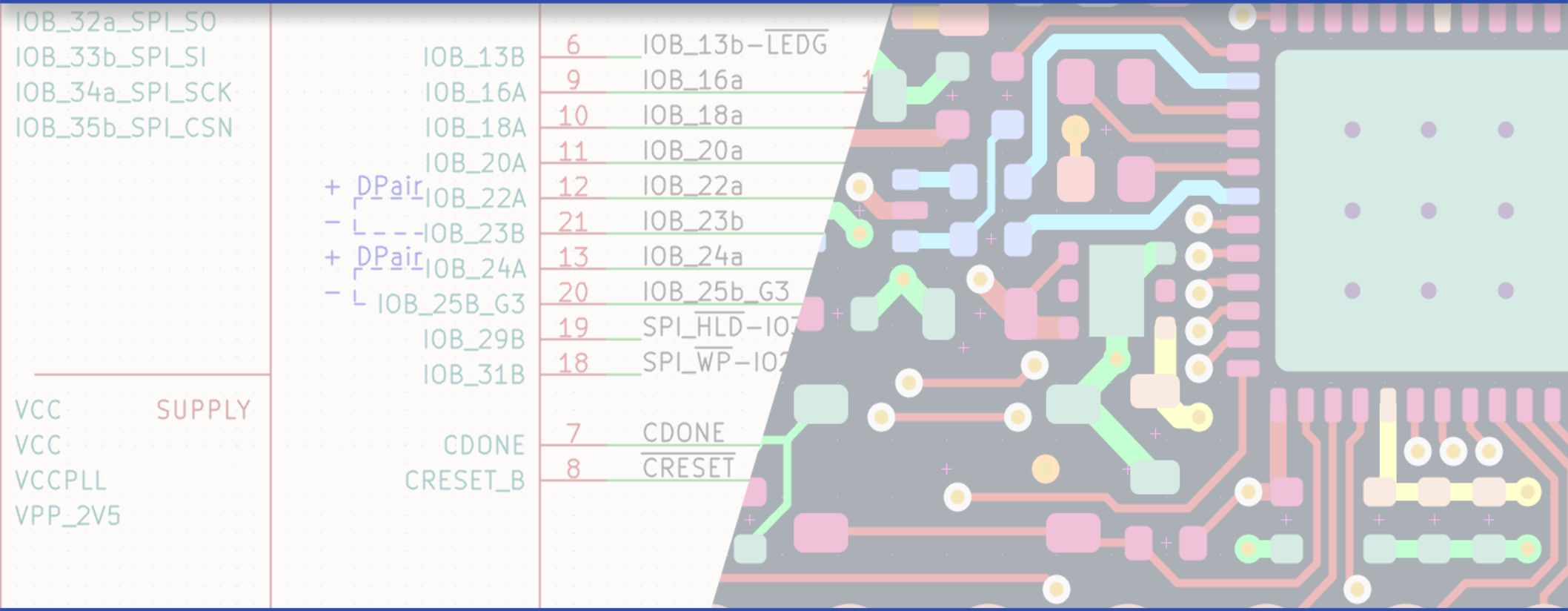


A SPICE simulation allows for:

- Time response analysis
- Frequency response analysis
- DC analysis
- Much more...

But we cannot model everything...

FEM: Finite Element Method



Maxwell's equations

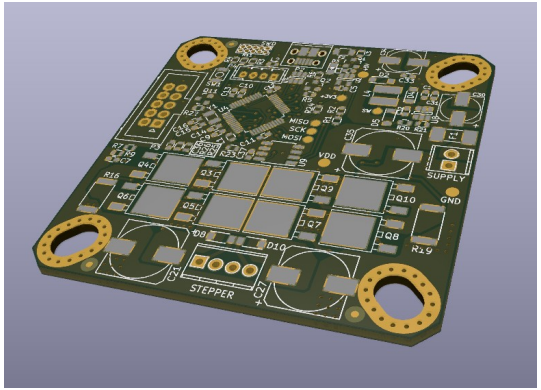
$$\nabla \cdot E = \frac{\rho}{\epsilon_0}$$ Electric charges contribute to the electric field

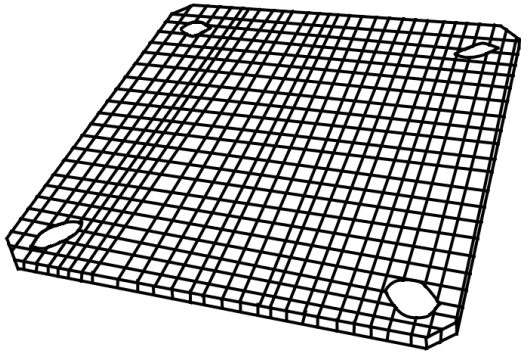
$$\nabla \cdot B = 0$$ There is no magnetic monopole

$$\nabla \times E = \frac{-\partial B}{\partial t}$$ A changing magnetic field creates an electric force

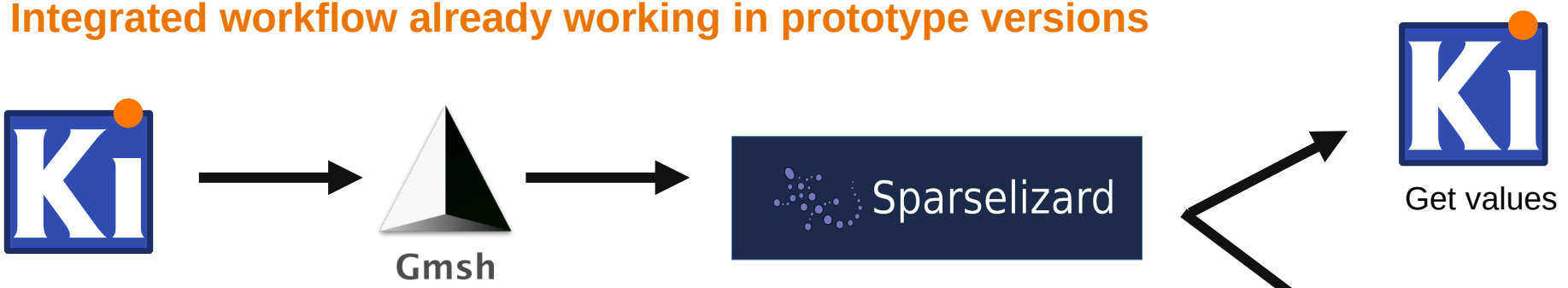
$$\nabla \times B = \mu_0 \left(J + \epsilon_0 \frac{\partial E}{\partial t} \right)$$ Electric currents create magnetic fields, a changing electric field behaves like a current

FEM: Slice the board into small domains, then solve Maxwell's equations on each domain





Integrated workflow already working in prototype versions



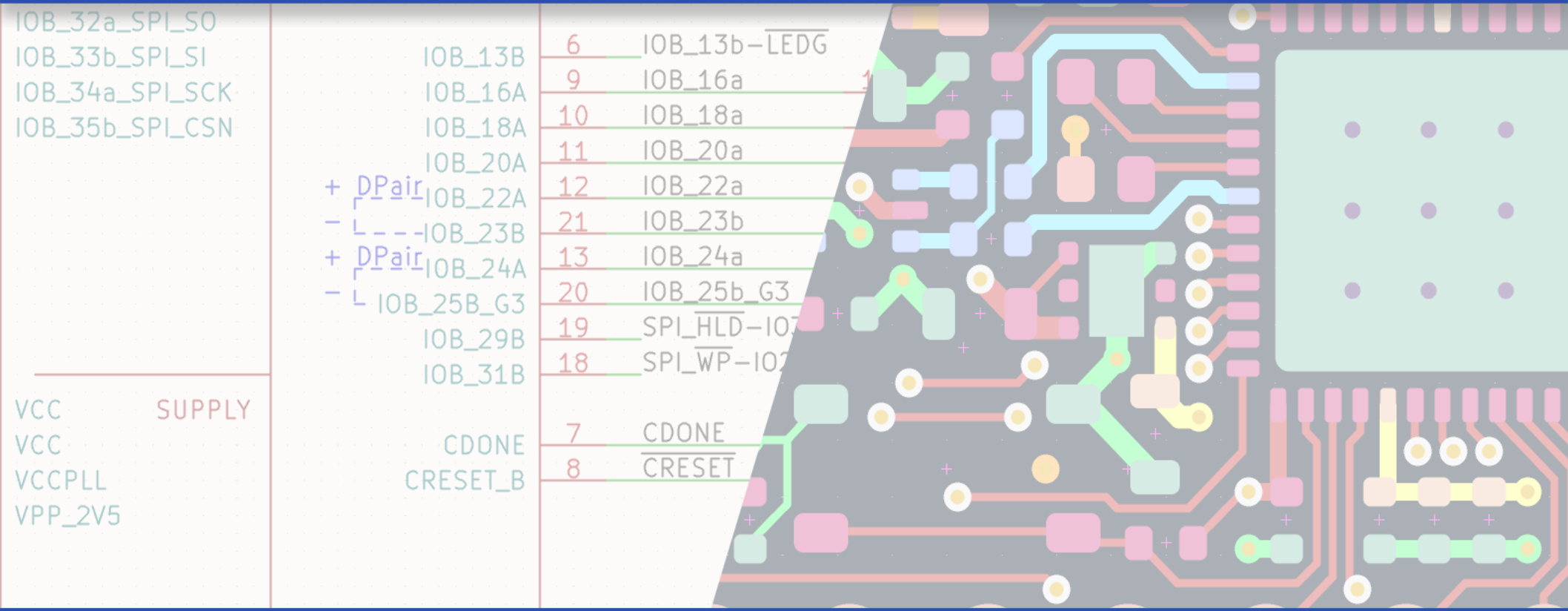
Board layout
Define objects of interest
Turn it into a geometry

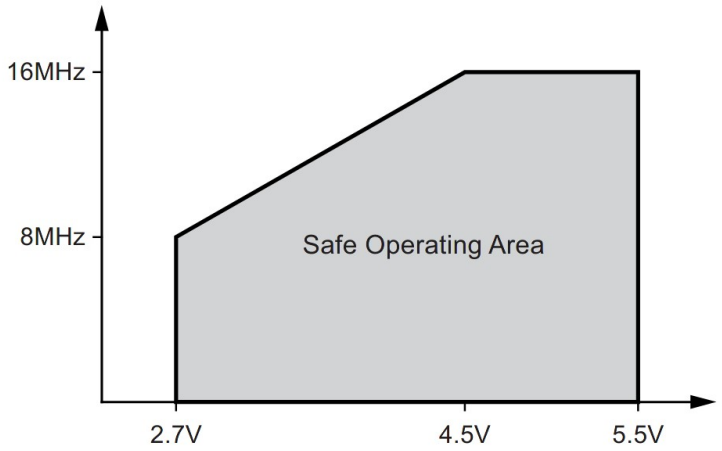
Create a mesh

Define EM equations
Solve equations
If needed, refine the mesh

Visualize output

Power integrity





(From the ATmega328P datasheet)

In the gray area, the device should work as expected
Outside, it may or may not work
We may face:

- A power off
- Resets
- Glitches

→ **We have to stay in the safe operating area**

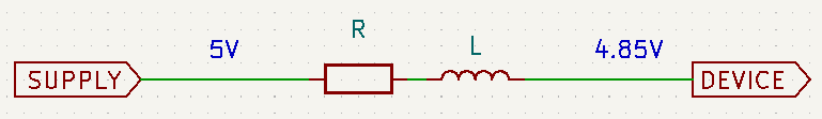
A good power integrity also helps with EMI
(Electromagnetic interference)

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Output Voltage (Note 12)	V_{OUT}	4.75	5.0	5.25	V	V_{IN} = 12V, I_{OUT} = 15mA
Line Regulation (Notes 12 & 13)	ΔV_{OUT}	—	33	220	mV	V_{IN} = 10V to 15V, I_{OUT} = 15mA
		—	400	700		V_{IN} = 7V to 60V, I_{OUT} = 15mA
		—	145	400		V_{IN} = 10V to 60V, I_{OUT} = 15mA
Temperature Coefficient	$\Delta V_{OUT}/\Delta T$	—	3.52	—	mV/°C	T_J = -40°C to +150°C V_{IN} = 12V, I_{OUT} = 15mA
Load Regulation (Notes 12 & 14)	ΔV_{OUT}	—	-20 -166	-130 -300	mV	I_{OUT} = 10mA to 20mA, V_{IN} = 12V I_{OUT} = 0.1mA to 50mA, V_{IN} = 12V

Voltage regulators are not perfect:

- DC voltage can be different from the nominal voltage
- The load regulation is not perfect



The power delivery network (PDN) is not perfect:

- The copper resistivity leads to a DC voltage drop
- Its inductance leads to a frequency-dependent voltage drop

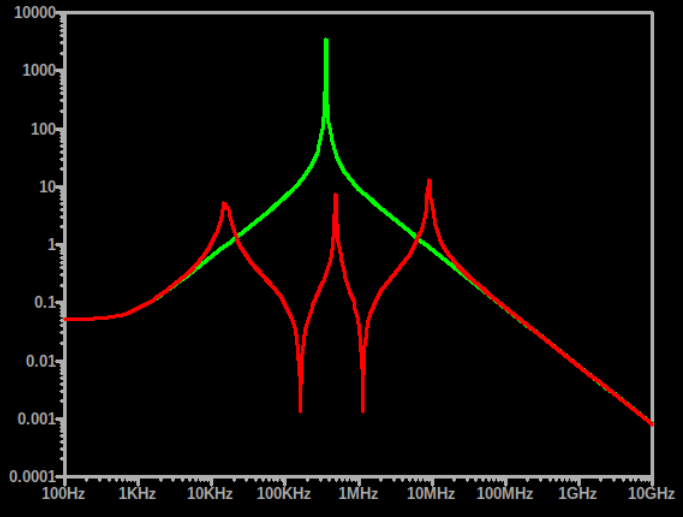
Power integrity: Mitigation

The voltage drop is U(f) = Z(f) . I (f)

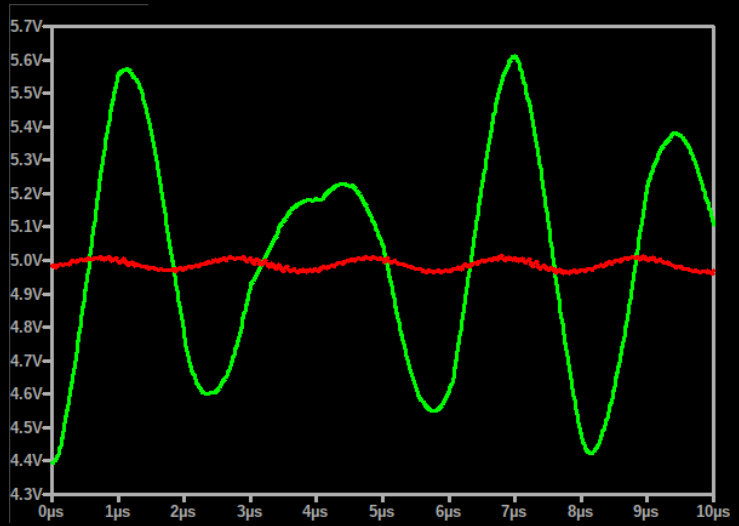
We want the voltage drop to be lower than a target voltage, Uo.
U (f) < Uo (f)
Which is equivalent the impedance being lower than a target impedance, Zo.
Z(f) < Zo (f)

The target impedance depends on the application

We add capacitors to lower the impedance. At high frequencies, we rely on the capacitance provided by the PCB itself



Impedance vs frequency



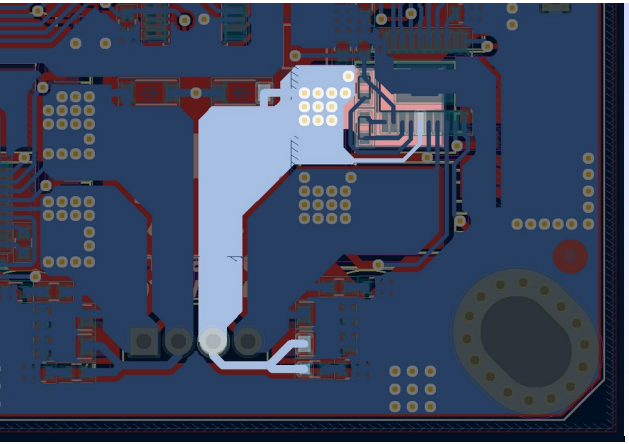
Voltage vs time

GREEN: without capacitor
RED: with capacitors

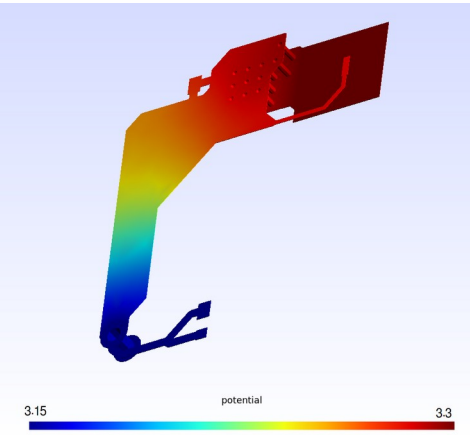
FEM: Application example – Voltage drop (3D)

Related applications:

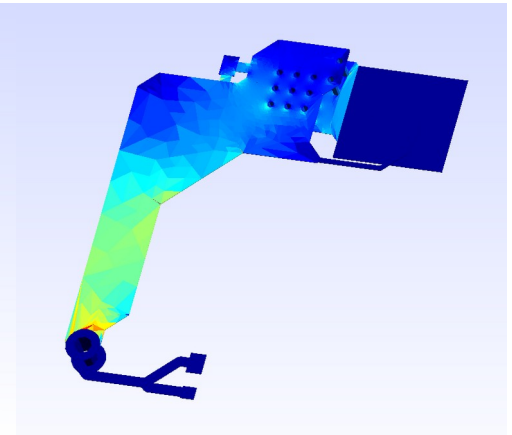
- Visualization of potential / current distribution
- Via stress analysis
- Resistance of complex geometries (copper zones)
- AC variant → Power delivery network impedance



PCB editor



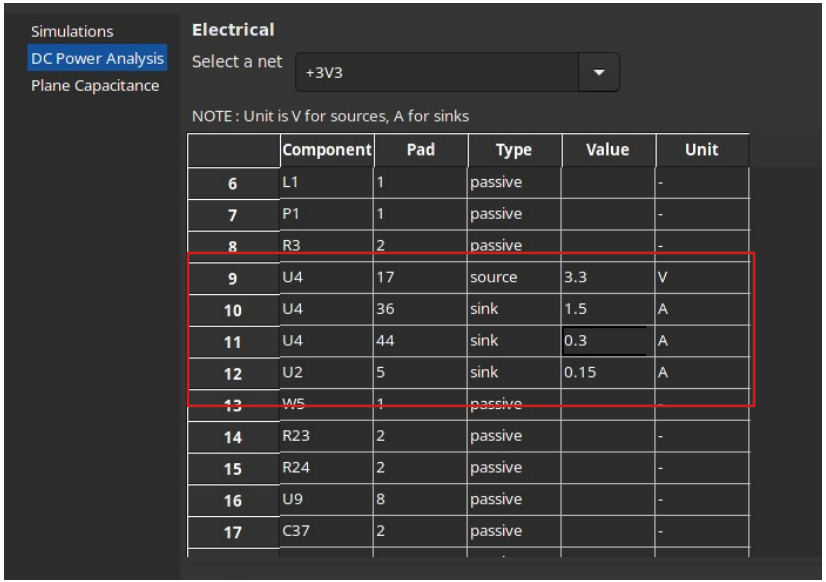
Electric potential



Current density

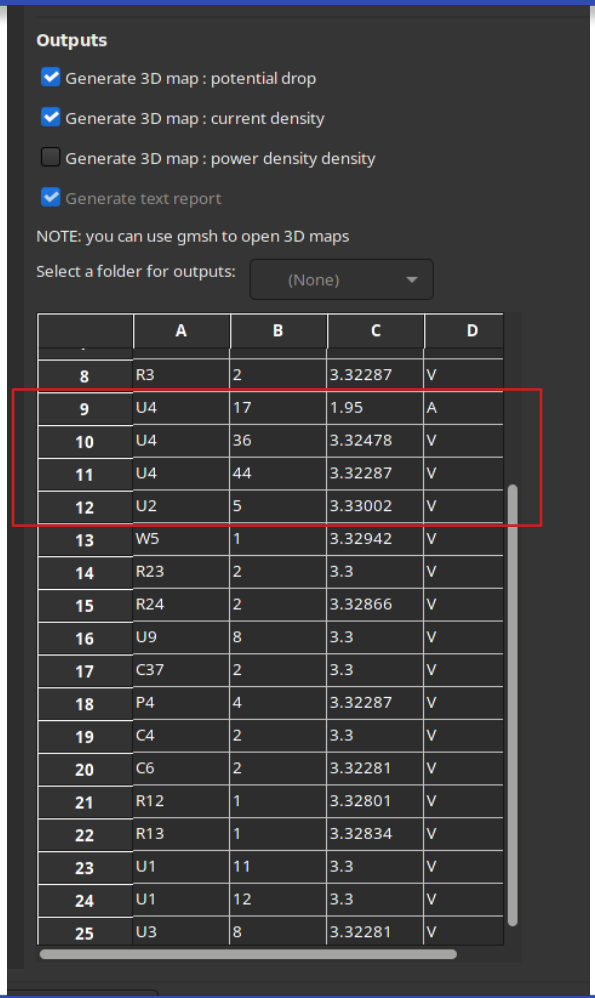
FEM: Application example – Voltage drop - Setup

The user chooses a net.
The user defines voltage sources and current sinks.
There can be multiple sources, and multiple sinks.



	Component	Pad	Type	Value	Unit
6	L1	1	passive		-
7	P1	1	passive		-
8	R3	2	passive		-
9	U4	17	source	3.3	V
10	U4	36	sink	1.5	A
11	U4	44	sink	0.3	A
12	U2	5	sink	0.15	A
13	W5	1	passive		-
14	R23	2	passive		-
15	R24	2	passive		-
16	U9	8	passive		-
17	C37	2	passive		-

(This GUI is for development purposes)

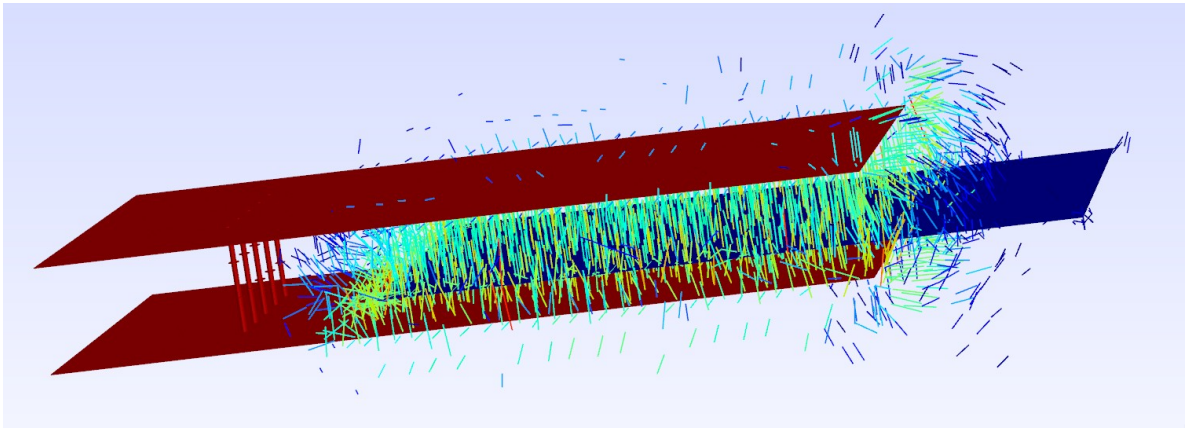


	A	B	C	D
8	R3	2	3.32287	V
9	U4	17	1.95	A
10	U4	36	3.32478	V
11	U4	44	3.32287	V
12	U2	5	3.33002	V
13	W5	1	3.32942	V
14	R23	2	3.3	V
15	R24	2	3.32866	V
16	U9	8	3.3	V
17	C37	2	3.3	V
18	P4	4	3.32287	V
19	C4	2	3.3	V
20	C6	2	3.32281	V
21	R12	1	3.32801	V
22	R13	1	3.32834	V
23	U1	11	3.3	V
24	U1	12	3.3	V
25	U3	8	3.32281	V

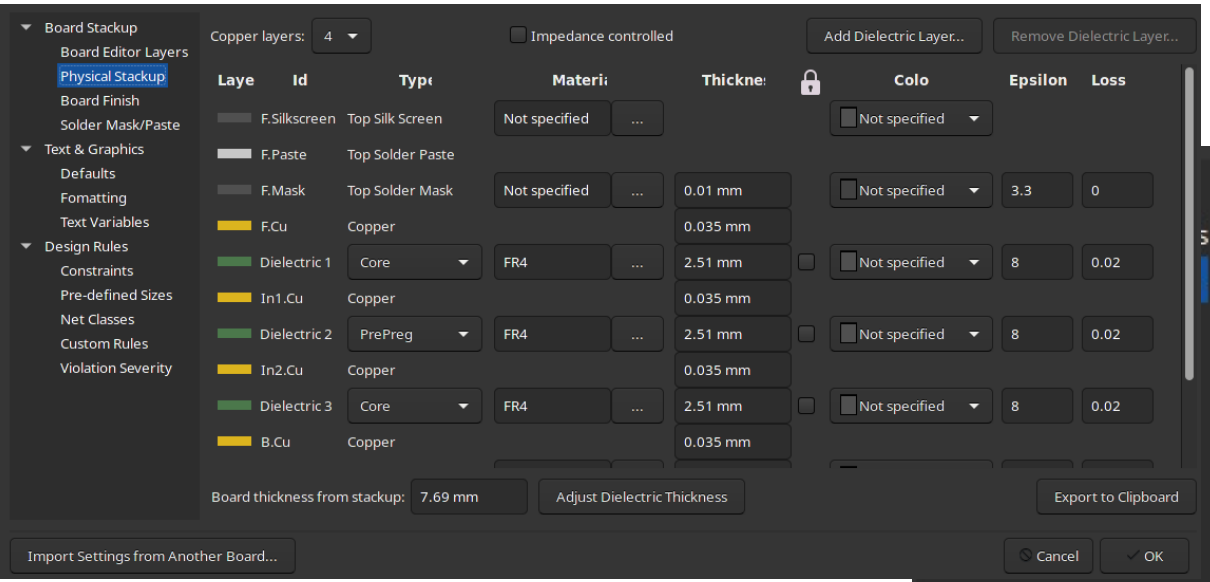
FEM: Application example – Capacitance

Related applications:

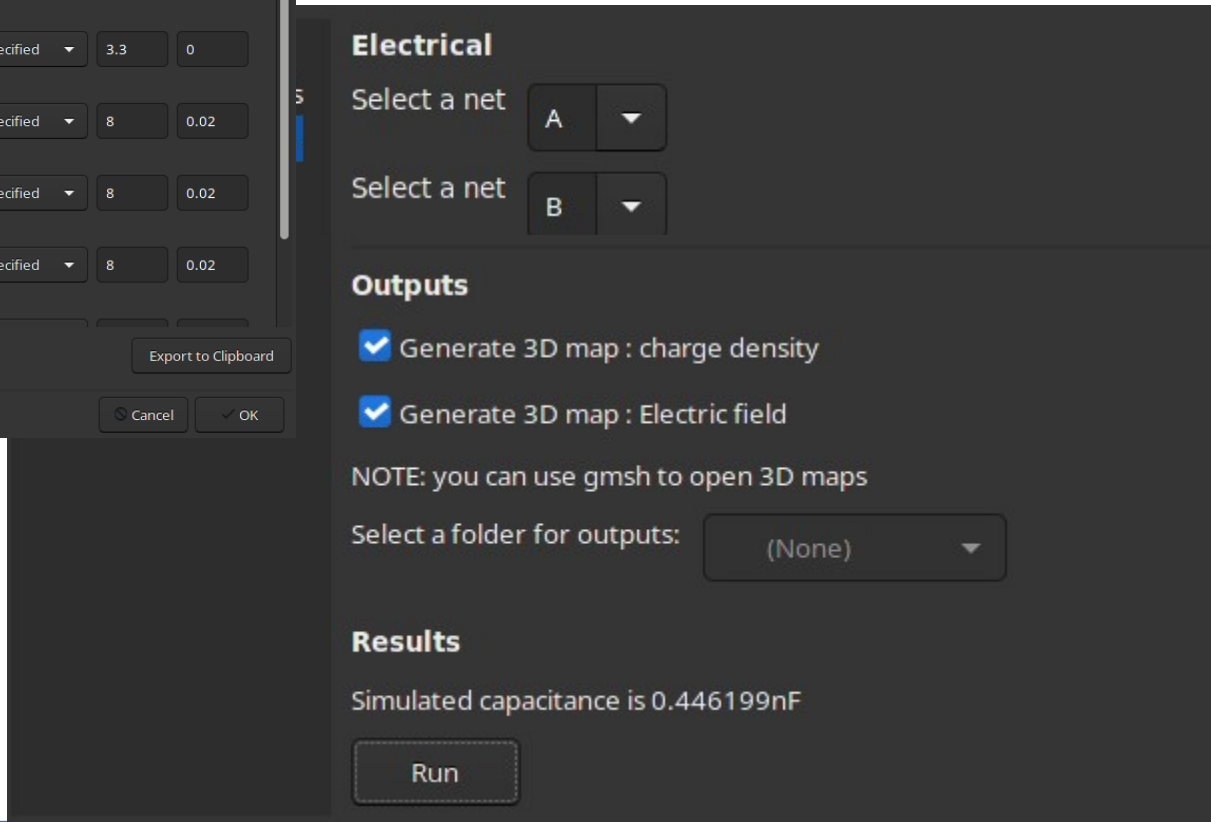
- Power integrity (plane capacitance)
- Some RF applications?



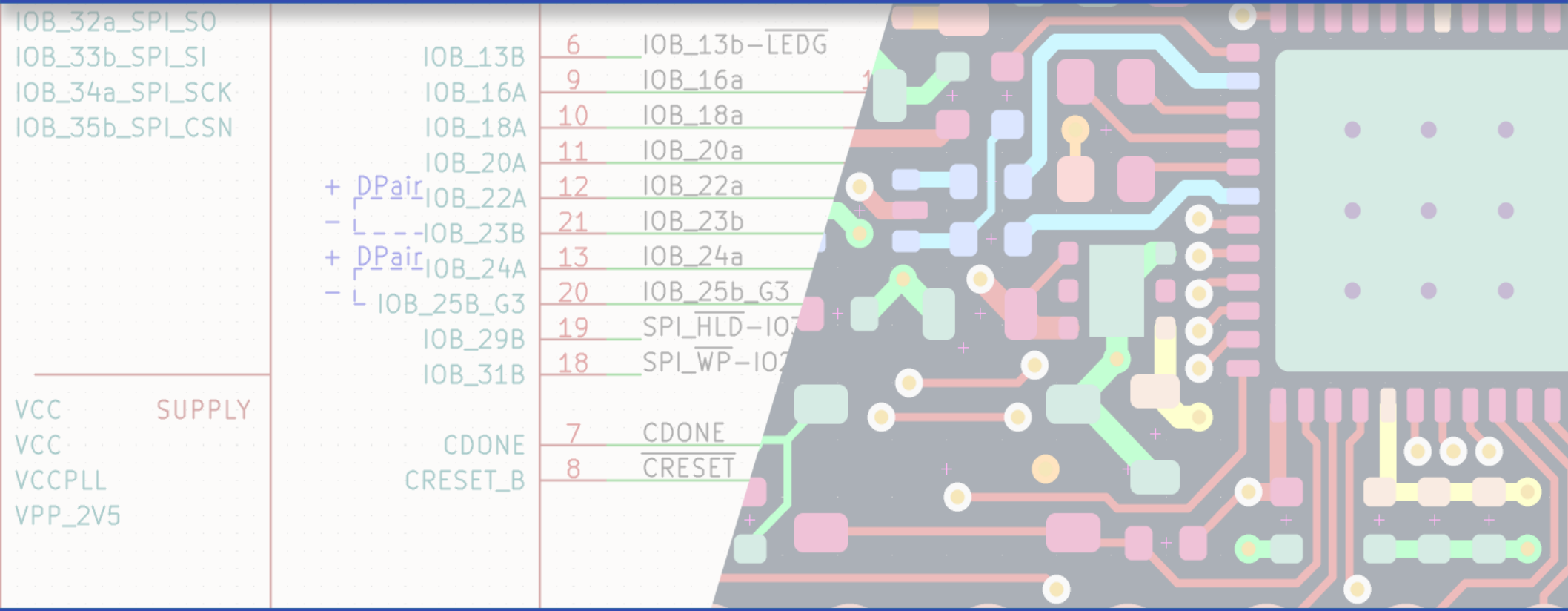
FEM: Application example – Capacitance - Setup



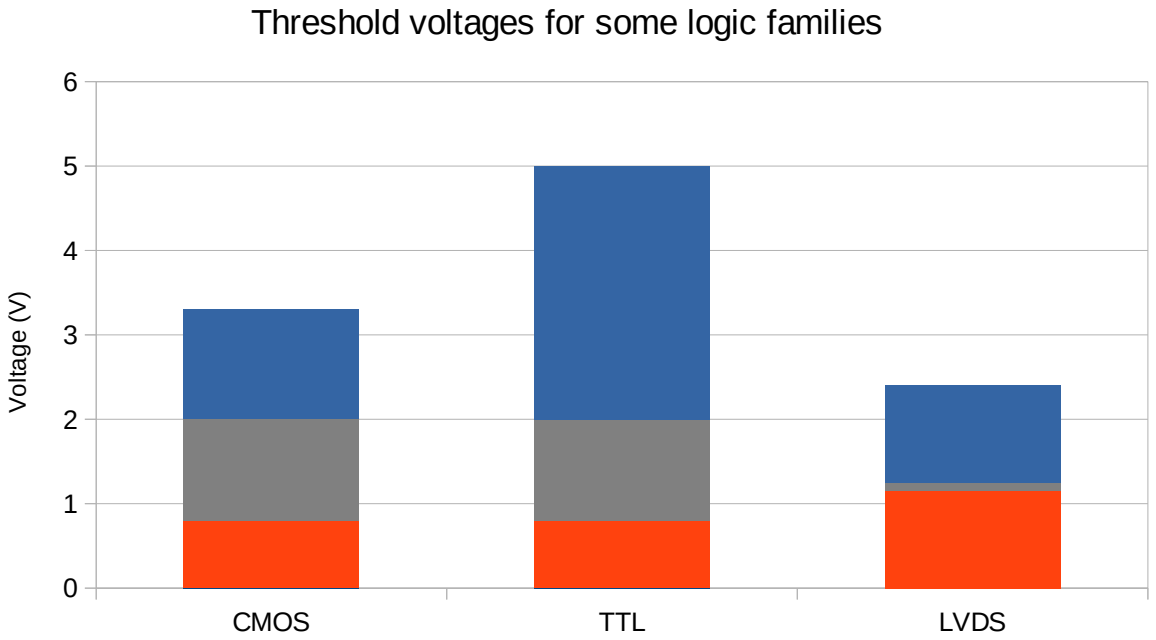
(This GUI is for development purposes)



Signal integrity

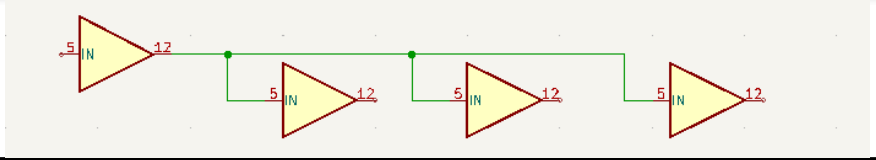


1s and 0s are digital information, and can only take two values.
We use analog signals to transmit bits which can take any value.
Between 1 and 0, there is always an undefined value.

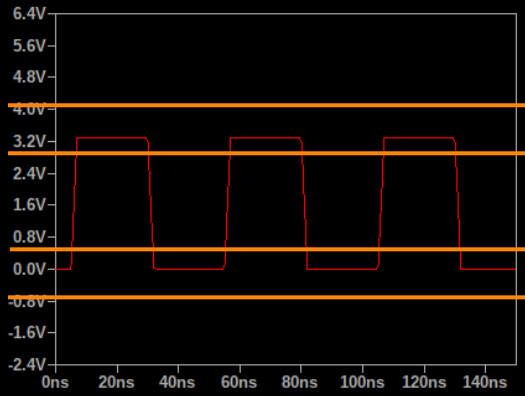


Blue: 1
Gray: undefined
Red: 0

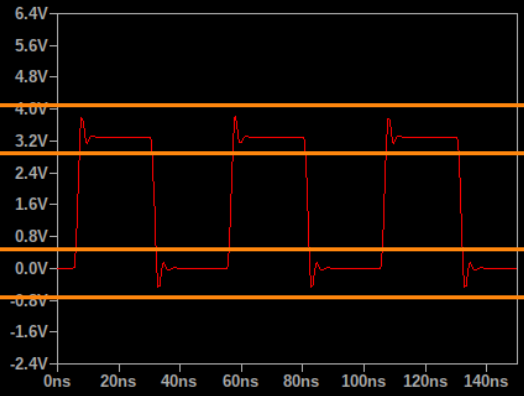
Signal integrity: what can go wrong



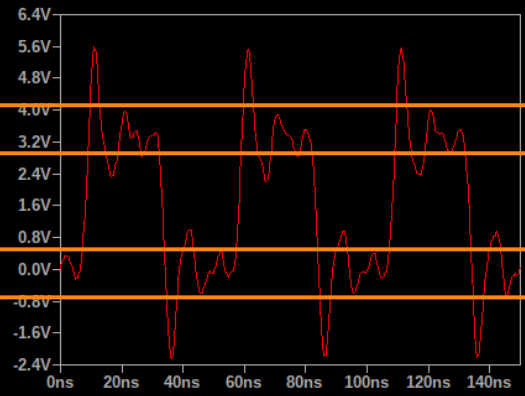
Intended signal



Simulated signal with components only



Simulated signal IBIS and PCB



Maximum voltage

Threshold for ‘1’

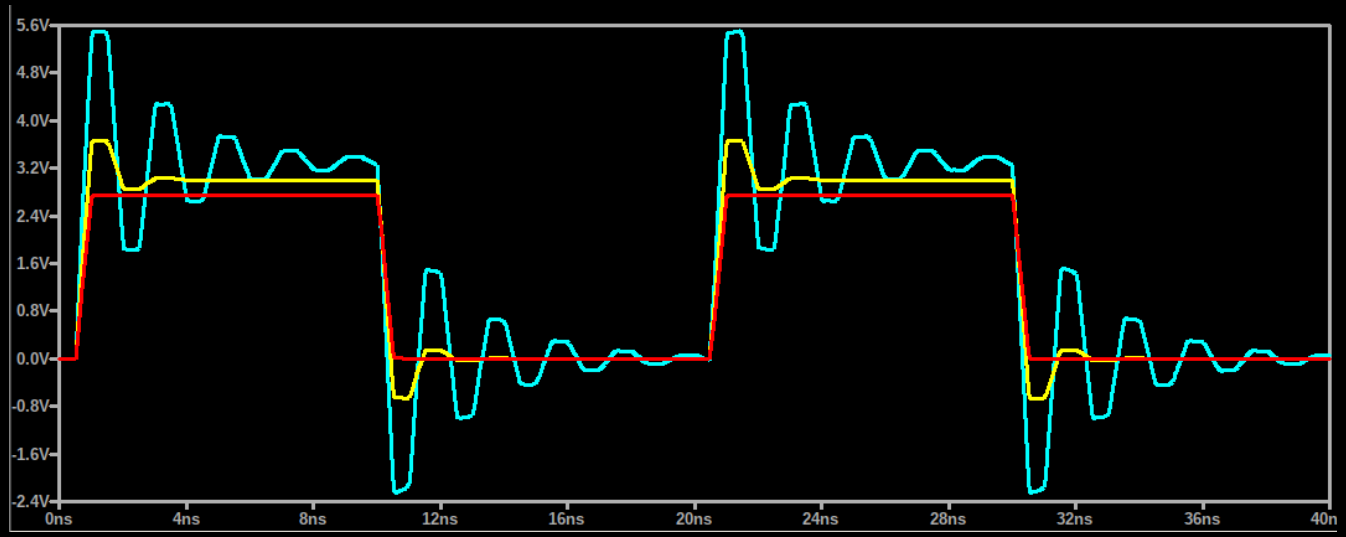
Threshold for ‘0’

Minimum voltage

Exceeding the safe voltage range of the component can deteriorate the component.
Crossing multiple times can lead to multiple captures.

FEM: Application example – Track impedance

Any track has a characteristic impedance defined by its capacitance and its inductance.
Maintaining a constant impedance is a key for signal integrity.
The receiver should match the track impedance.
This is not a high-frequency problem, but a low rise time problem.



Blue: 0 % matching
Yellow: 66 % matching
Red: 100 % matching

FEM: Application example – Track impedance - Setup

Substrate Parameters

εr:	4.4	...
tan δ:	0.01	...
ρ:	1.72e-8	...
H:	0.2	mm
H(top):	1e+20	mm
T:	0.035	mm
Roughness:	0	mm
μ(substrate):	1	
μ(conductor):	1	

Component Parameters

Frequency:	1	GHz

Physical Parameters

W:	0.2	mm
L:	27.0806	mm

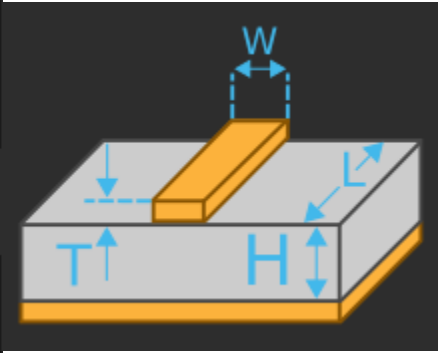
↓ Analyze Synthesize ↑

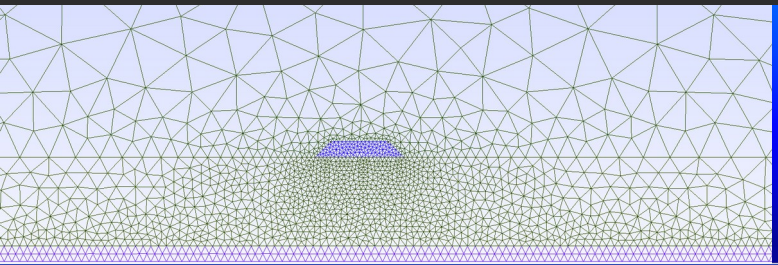
Electrical Parameters

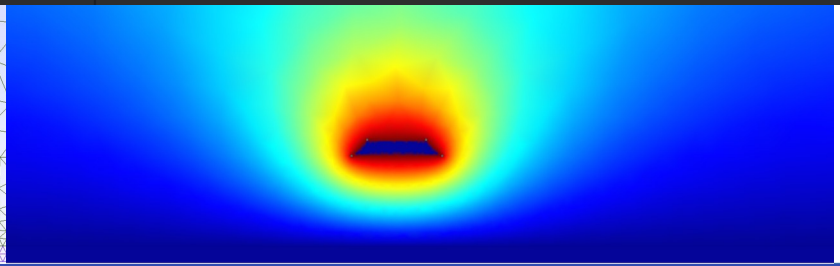
Z0:	67.5835	Ω
Ang_l:	0.964479	rad

Results

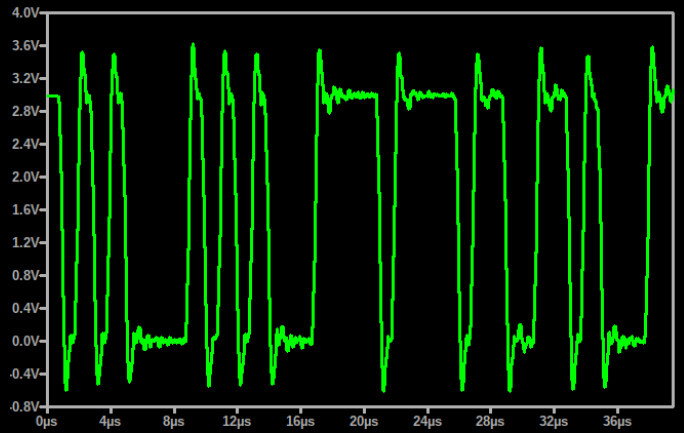
Effective εr:	2.88769
Conductor losses:	0.0850437 dB
Dielectric losses:	0.0354279 dB
Skin depth:	2.0873 μm



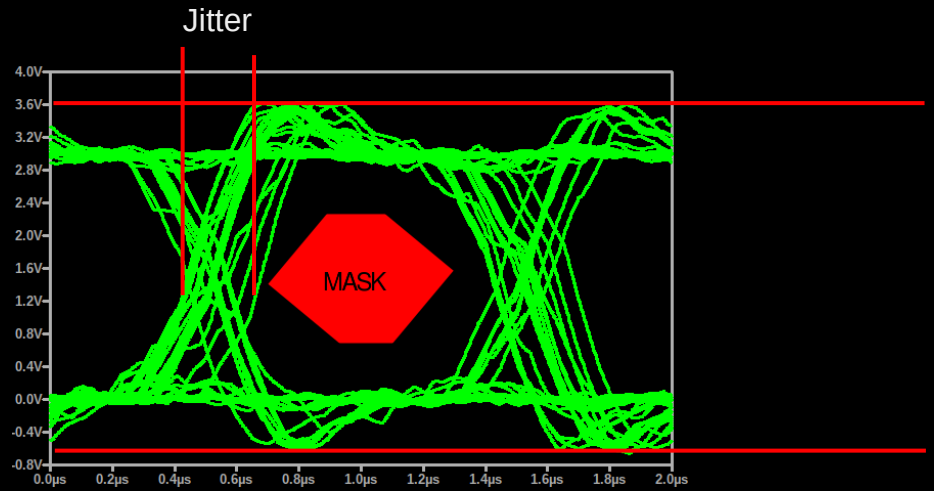




Signal Integrity: Eye diagram



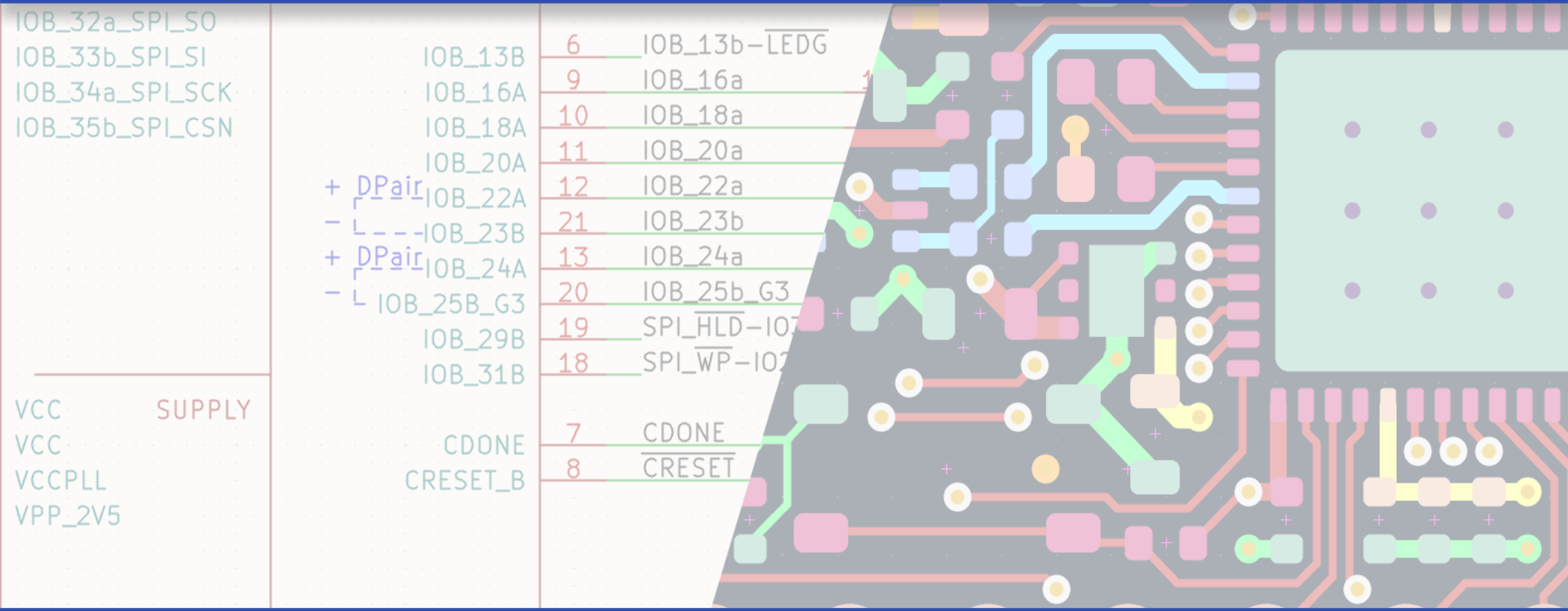
Time plot



Eye diagram

The eye diagram is a compliance test
Using a random sequence, we can measure the ISI (inter symbol interference)
The signal should not enter the mask

IBIS: I/O Buffer Information Specification

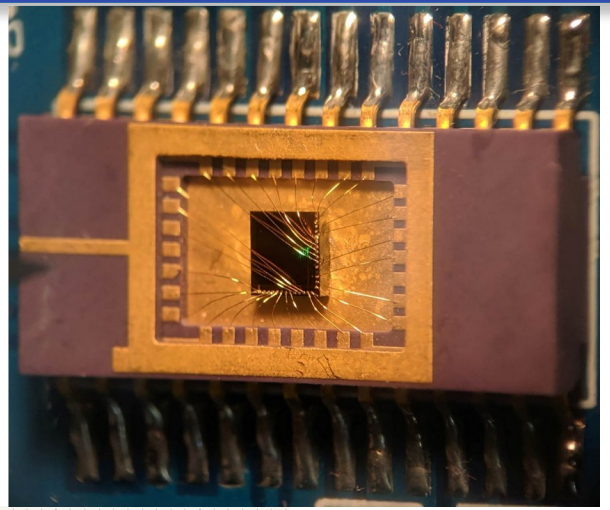


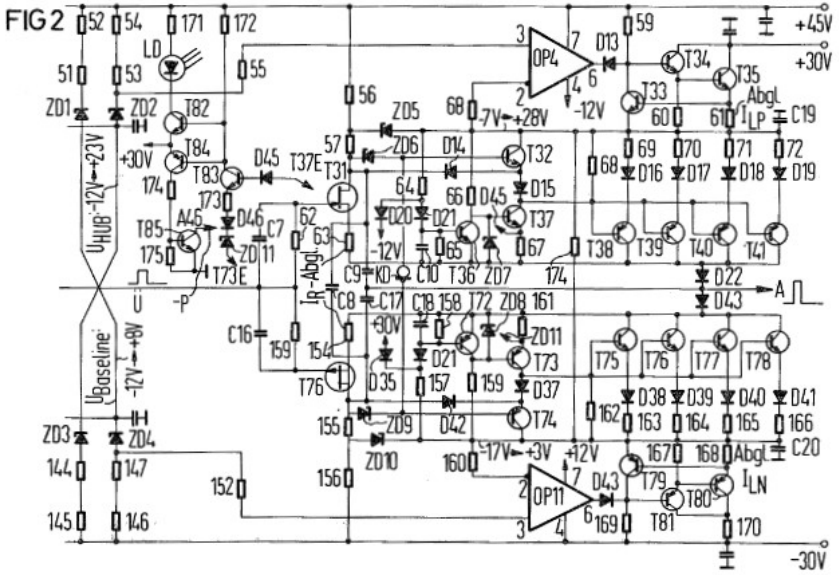
What is IBIS?

- IBIS (IO Buffer Information Specification) is a open file format (ibis.org)
- It is not a model, but an electrical description of a component
- Manufacturers are reluctant to provide SPICE models
- We can infer a working SPICE model from it
- There is a lot of information that can be extracted:
  - Push / pull transistor characteristics
  - Imbalance in transistors / differential pairs
  - Die capacitance
  - Pin capacitance, inductance and resistance
  - Much more

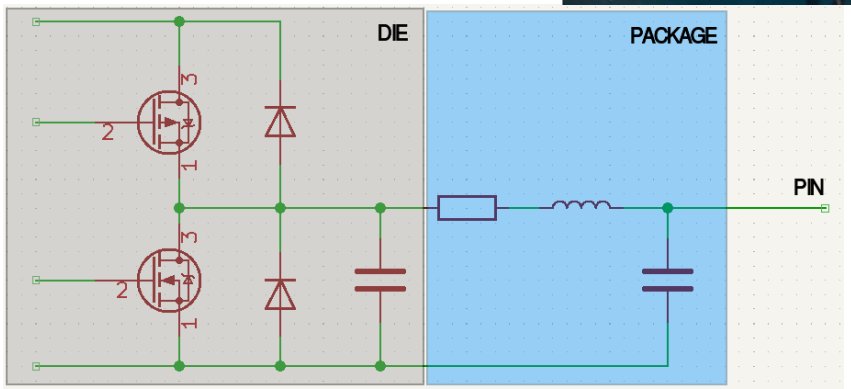
IBIS: Behavioral model

An output / input stage can be complex with a lot of components
A model derived from an IBIS description is a lot faster than a full SPICE model





A push-pull output, patent US4329728A, expired



Model that can be used for all IBIS descriptions

IBIS file formats

.ibs
die
(+package)

.pkg
package

.ebd
PCB

.ims
interconnect

.ami
algorithms

What manufacturers usually give

In this presentation

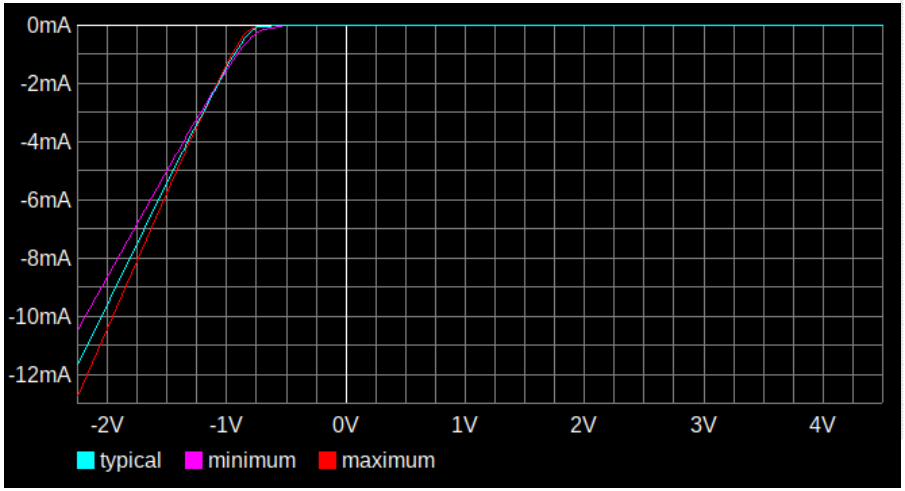
IBIS: What is inside? R, L, C, and diodes

Package parasitic values
(can be defined for individual pins)

```
[Package]          |20 TSSOP - PW package

                   typ              min              max
R_pkg              0.05             0.04             0.06
L_pkg              1.0nH            0.8nH            1.2nH
C_pkg              0.2pF            0.16pF           0.24pF
```

Diodes: Current VS voltage tables (IV tables)



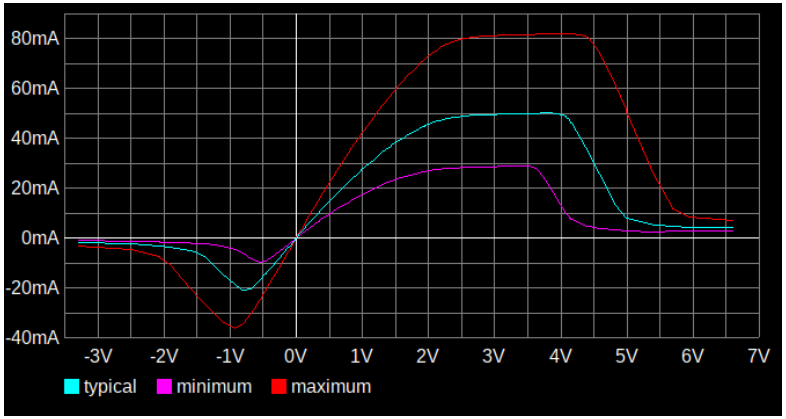

```
[GND Clamp]

   Voltage         I(typ)           I(min)           I(max)

   -2.25           -0.0117097       -0.0104769       -0.0127448
   -1.41975        -0.0047652       -0.00441769      -0.00501465
   -1.413          -0.00470981      -0.0043696       -0.00495297
   -1.36575        -0.00432299      -0.00403394      -0.00452237
   -1.359          -0.00426788      -0.00398614      -0.00446105
   -1.3455         -0.00415777      -0.00389066      -0.00433856
   -1.33875        -0.00410277      -0.00384298      -0.00427739
   -1.1565         -0.00263819      -0.00257621      -0.00265617
   -1.116          -0.00232029      -0.00230204      -0.00230743
   -1.10925        -0.00226769      -0.0022567       -0.00224985
   -0.9675         -0.00120242      -0.00133869      -0.00108784
   -0.96075        -0.00115444      -0.0012972       -0.00103574
   -0.954          -0.00110684      -0.001256        -0.000984111
   -0.94725        -0.00105963      -0.00121509      -0.000932982
   -0.9405         -0.00101284      -0.00117448      -0.000882401
   -0.93375        -0.000966507     -0.00113421      -0.000832418
   -0.927          -0.000920657     -0.00109428      -0.000783091
   -0.8595         -0.000498419     -0.000718766     -0.000345923
   -0.85275        -0.000461118     -0.000684198     -0.000310834
   -0.846          -0.000425021     -0.000650307     -0.000278063
```

IBIS: What is inside? Transistors and waveforms

Transistor: Current VS voltage tables (IV tables)

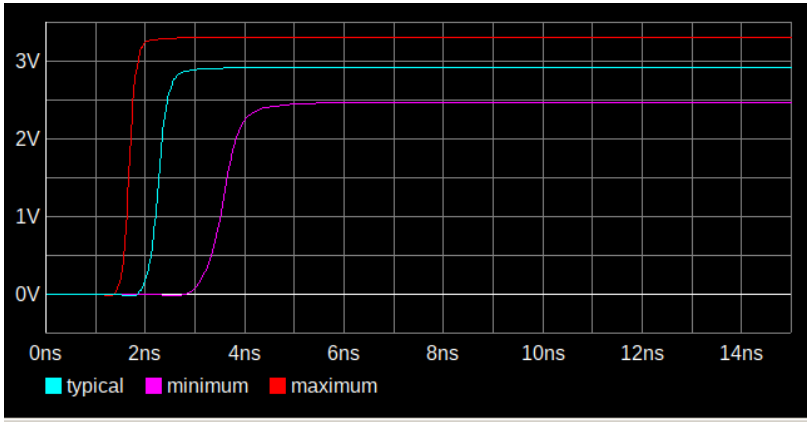



```
[Pullup]

    Voltage         I(typ)          I(min)          I(max)

    -3.3            0.00368743      0.0022396       0.00612904
    -1.9437         0.00406909      0.00199612      0.00829478
    -1.9338         0.00409011      0.00200156      0.00838743
    -1.7853         0.00445501      0.00209925      0.0107052
    -1.5972         0.00527086      0.00228445      0.0158986
    -1.5873         0.00533356      0.00229686      0.0161797
    -1.4388         0.00671665      0.00252971      0.0203398
    -1.3794         0.0076292       0.0026544       0.0219614
    -1.0725         0.0151185       0.00387742      0.0293573
    -1.0626         0.0153564       0.00394487      0.0295344
    -1.0527         0.0155912       0.00401522      0.0297034
    -0.9438         0.0179119       0.00504043      0.0306617
    -0.8151         0.0193948       0.00707632      0.0288613
    -0.6765         0.0175485       0.00940493      0.0248755
```

Waveforms (VT tables)




```
[Rising Waveform]
V_fixture = 0V
V_fixture_min = 0V
V_fixture_max = 0V
R_fixture = 3000hm
C_fixture = 0F

    Time            V(typ)          V(min)          V(max)

    0               6.73865e-06     1.02646e-05     3.59424e-06
    1.04121e-09     0.000830126     0.00052498      0.00119797
    1.30809e-09     0.00104118      0.000656913     -0.0183515
    1.31583e-09     0.0010473       0.000660741     -0.0176304
    1.34039e-09     0.00106672      0.000672879     -0.00852587
    1.37773e-09     -0.000967699    0.000691341     0.00532204
    1.43632e-09     -0.00415911     0.000720303     0.070565
    1.44917e-09     -0.00485906     0.000726655     0.0918659
    1.46359e-09     -0.00564476     0.000733785     0.119353
    1.50117e-09     -0.0076919      0.000752363     0.212438
    1.53949e-09     -0.00977912     0.000771305     0.350849
    1.55188e-09     -0.010454       0.000777429     0.408408
```

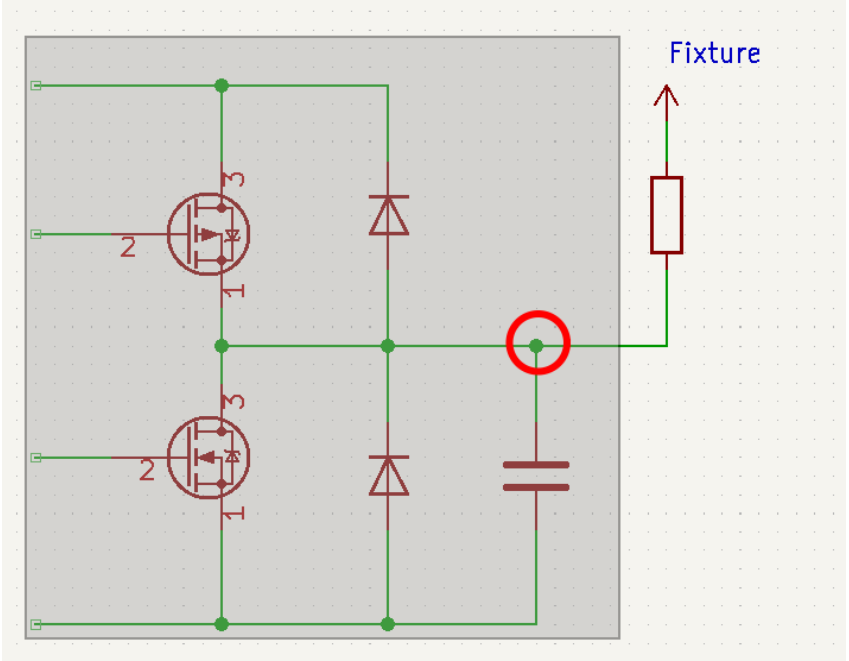
We don’t have transient information for the transistors

Falling / rising waveforms are given for a specific load with a fixture voltage (usually VCC or GND)

We apply time dependent Ku/Kd modifiers to the transistor IV tables. (1: current flowing, 0: no current flow)
=> Two unknowns

At the point in red, the sum of currents is equal to zero.
=> One equation

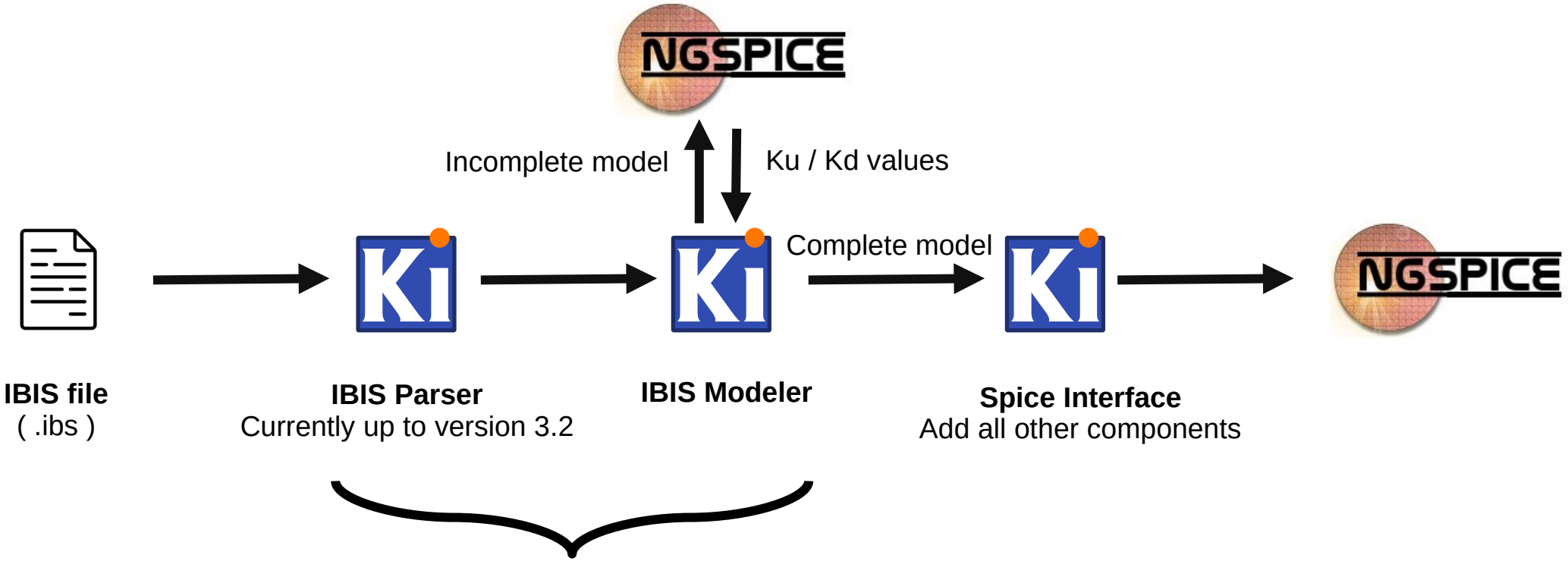
We can have two rising /falling waveforms with two different fixtures.
=> One equation



With 2 unknown and 2 equations, we can easily solve for Ku / Kd
With 2 unknown and 1 equations, we have to assume simultaneous switching (Kd = 1 – Ku)

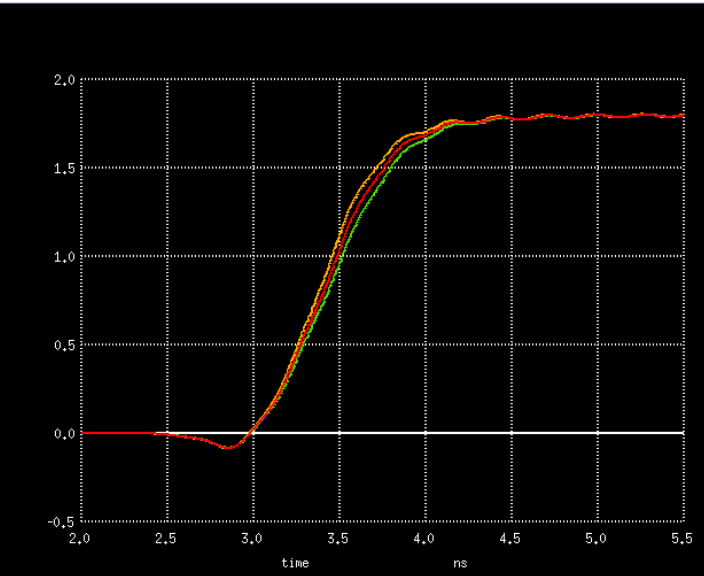
We need to build a spice model for each bitstream we want to use

IBIS: Building a model from KiCad

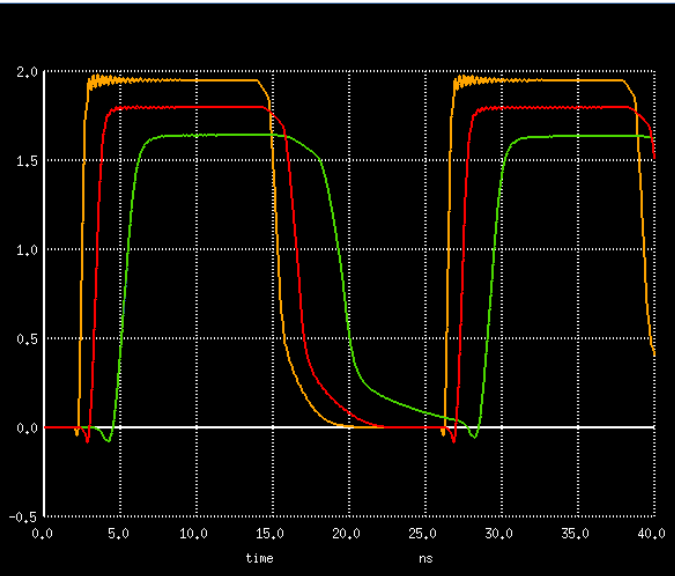


IBIS: Simulation examples (SN74HCS244)

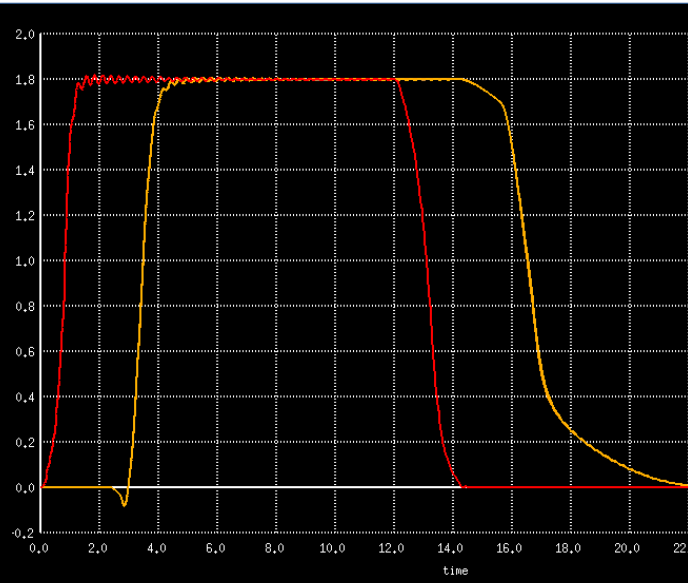
Package parasitics
Can vary from a chip to another



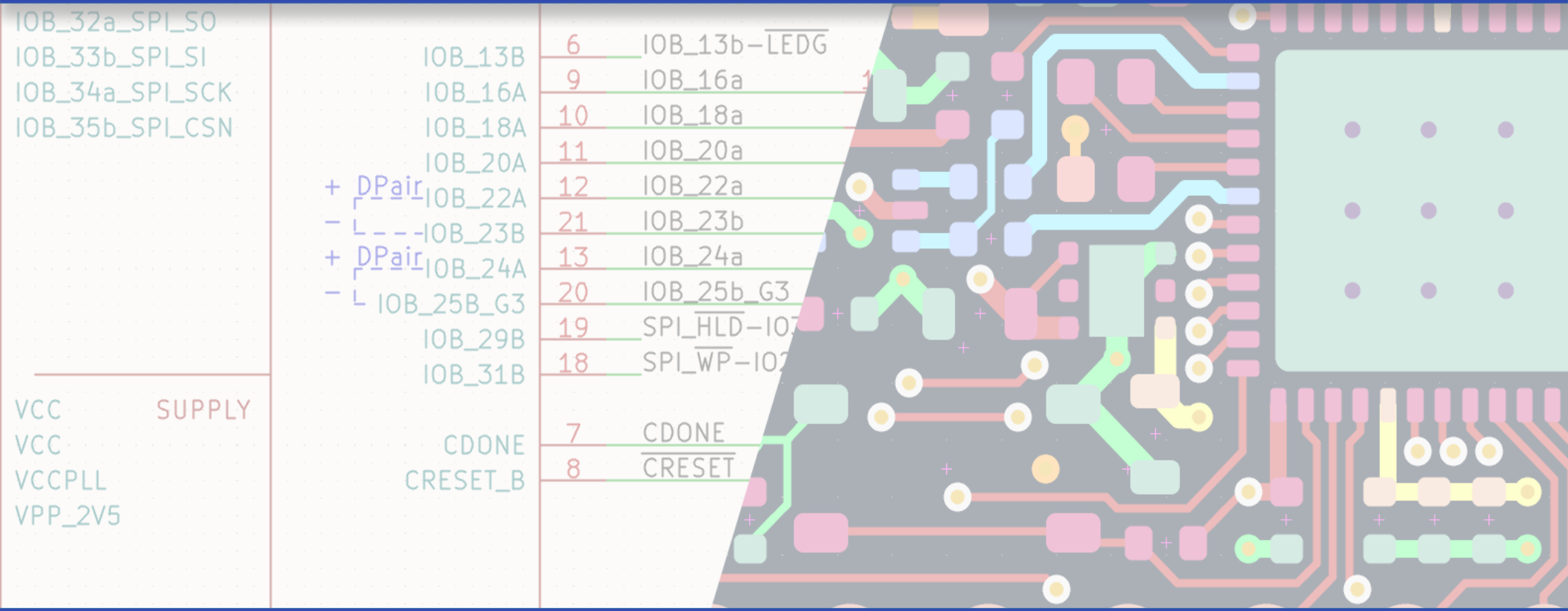
Supply voltage
Typical, minimum and maximum behaviors are defined



Modeling accuracy
(Red: 0 waveform pairs)
(Yellow: 2 waveform pairs)



Conclusion


IOB_32a_SPI_SO
IOB_33b_SPI_SI
IOB_34a_SPI_SCK
IOB_35b_SPI_CSN
VCC SUPPLY
VCC
VCCPLL
VPP_2V5
IOB_13B
IOB_16A
IOB_18A
IOB_20A
+ DPair IOB_22A
− IOB_23B
+ DPair IOB_24A
− IOB_25B_G3
IOB_29B
IOB_31B
CDONE
CRESET_B
6 IOB_13b−LEDG
9 IOB_16a
10 IOB_18a
11 IOB_20a
12 IOB_22a
21 IOB_23b
13 IOB_24a
20 IOB_25b_G3
19 SPI_HLD−IO
18 SPI_WP−IO
7 CDONE
8 CRESET

- New ways to model things
  - IBIS support
  - New transmission lines topologies in PCB calculator (eg: differential stripline)

- New simulations accounting for the actual layout:
  - Via stress analysis
  - Power integrity analysis
  - Signal integrity analysis
  - Crosstalk analysis

- New features:
  - Auto-track width to maintain a constant characteristic impedance
  - New DRC rules based on PI / SI
  - Add measurements of track delay, capacitance, resistance, etc..

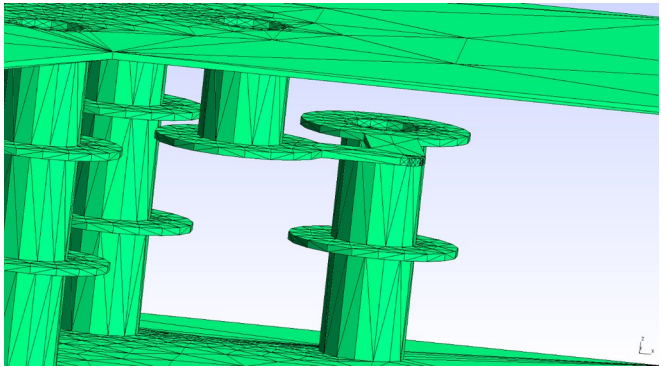
But it’s a long road...

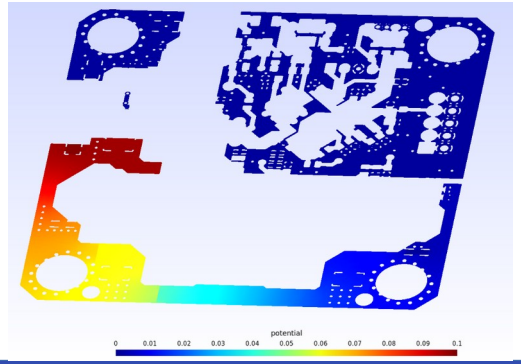
Conclusion:

- KiCad would benefit from advanced simulation capabilities
- Power and signal integrity simulations need PCB simulations
- FEM provides a way to extract information to get a SPICE model
- IBIS provides a way to get accurate and fast SPICE models

Special thanks to:

- Thomas Pointhuber (KiCad)
- Alexandre Halbach (Sparselizard)
- Holger Vogt (ngspice)
- The KiCad team





Thank you for attention