

# Hardware Based CPU Undervolting on The Cheap

Stealing Your Secrets for \$30

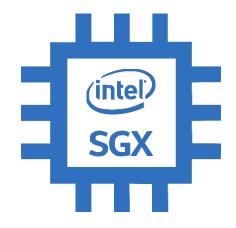
Zitai Chen, Georgios Vasilakis, Kit Murdock, David Oswald, Flavio D. Garcia

University of Birmingham, UK

# TEES

#### Trusted Execution Environments







AMD Secure Processor



#### Threat Model

#### What are some of the use cases for Intel® SGX?

Intel® SGX allows you to run applications on untrusted infrastructure (for example public cloud) without having to trust the infrastructure provider with access to your applications.

Source: Fortanix Intel SGX https://web.archive.org/web/20201001235308/https://fortanix.com/intel-sgx/

#### **Enarx threat model**

Enarx is built with these principles in mind:

- · Don't trust the host
- · Don't trust the host owner
- · Don't trust the host operator
- · All hardware cryptographically verified
- · All software audited and cryptographically verified

Source: Enarx Threat Model https://github.com/enarx/enarx/wiki/Threat-Model

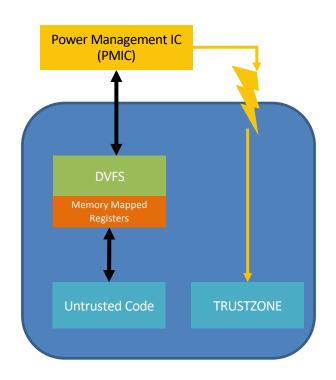
- Untrusted OS
- Untrusted owner
- Untrusted Infrastructure

Enable applications to define secure regions of code and data that maintain confidentiality even when an attacker has physical control of the platform and can conduct direct attacks on memory.

Source: Intel® SGX for Dummies (Intel® SGX Design Objectives) https://software.intel.com/content/www/us/en/develop/blogs/protecting-application-secrets-with-intel-sgx.html

#### Fault injection - ARM

### **ARM SoC**





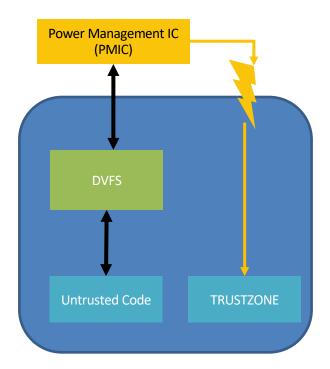
Adrian Tang et al. "CLKSCREW: exposing the perils of security-oblivious energy management"
In: USENIX Security Symposium. 2017



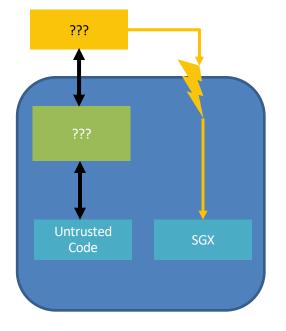
Pengfei Qiu et al. "VoltJockey: Breaching TrustZone by Software-Controlled Voltage Manipulation over Multi-core Frequencies"

In: CSS. 2019

# **ARM SoC**



# Intel





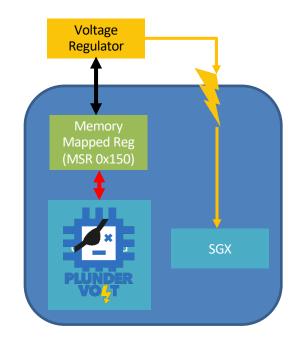


- Faulting Multiplication
- Faulting RSA in SGX
- Faulting AES-NI in SGX
- Memory Corruption

Kit Murdock et al. Plundervolt: Software-based Fault Injection Attacks against Intel SGX

In: 41st IEEE Symposium on Security and Privacy (S&P'20)

# Intel



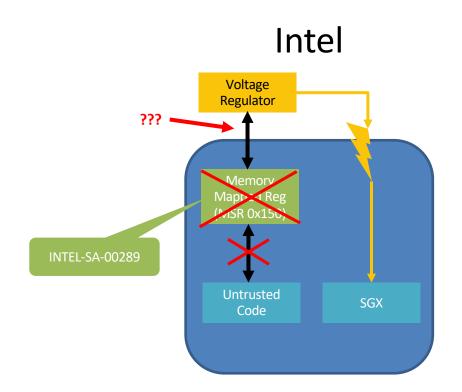
#### Undervolting via MSR 0x150 disabled



## Undervolting via MSR 0x150 disabled

#### Recommendations:

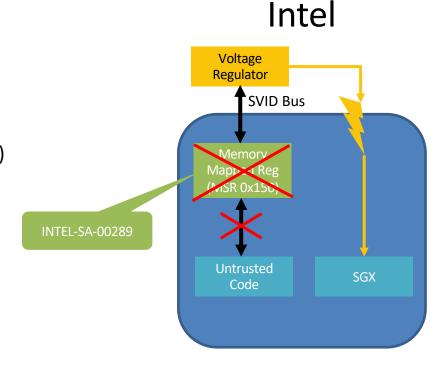
Intel recommends that users of the above Intel® Processors update to the latest BIOS version provided by the system manufacturer that addresses these issues.



#### SVID Bus

#### **SVID Bus**

- 3 Wire interface
  - CLK, DATA and ALERT(Not required)
- Clock @ 25MHz
- Logical High >0.64V, Low <0.45V</li>





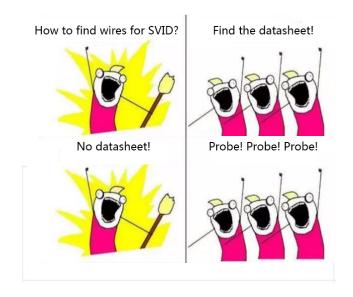
1. L6751C Digitally controlled dual PWM for Intel VR12 and AMD SVI

2. 8th Generation Intel® CoreTM Processor Families Datasheet, Volume 1 of 2



#### SVID Bus – Which wire?

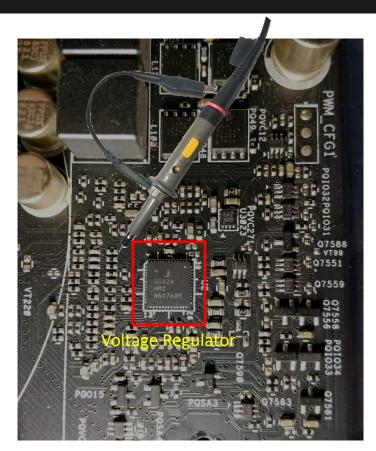


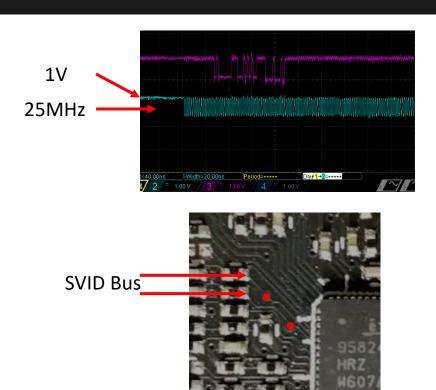


- 1\*A4 page long
- Does not show pin definition
- No information about the signal



#### SVID Bus – Which wire?

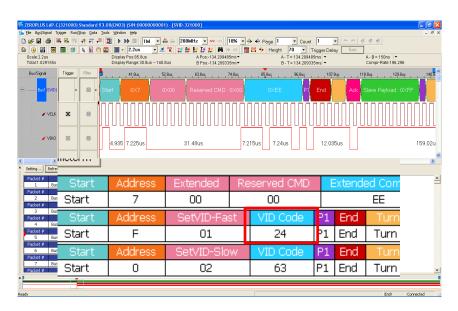






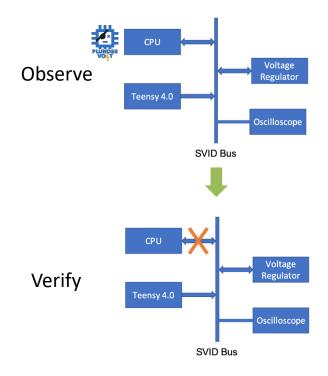
#### **SVID Protocol**

#### **Commands & Packet Strucutres**



Src: ZEROPLUS Protocol Analyzer SVID\_V1.04.0 [Link]

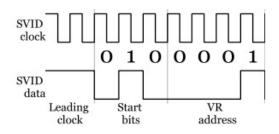
#### **RE Voltage Identifiers**





#### **SVID Protocol**

#### SVID signals and data frame



010	address 0000/0001	command 00001	voltage ID	parity	01	1
0	3	7	12	20	21	24

status ok: 01 error: 10	response 0000/0001	pari	ity
0 2		6	7

VID: 1byte, computed as (voltage U in volt):

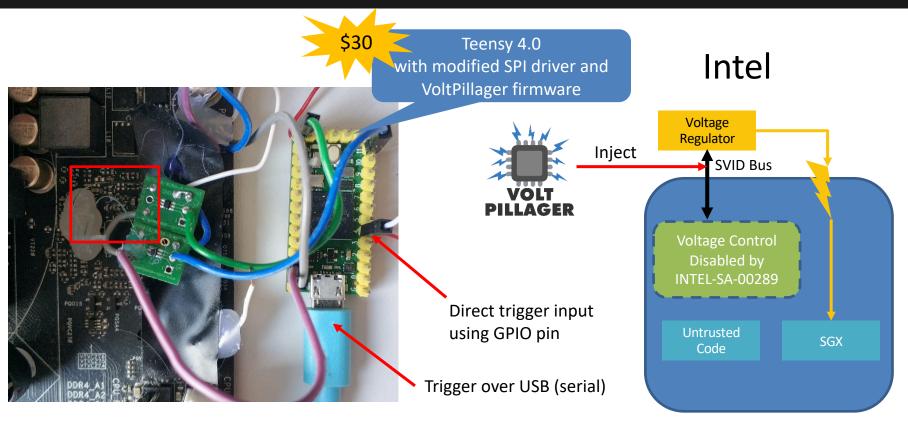
$$VID = \left| \frac{U - 0.245}{0.005} \right|$$

VID Commands: 5bits

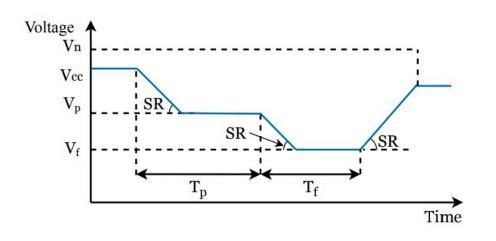
Command name	Value
Extended	0x00
SetVID-Fast	0x01
SetVID-Slow	0x02
SetVID-Decay	0x03
$\operatorname{SetPS}$	0x04
$\operatorname{SetRegADR}$	0x05
SetRegDAT	0x06

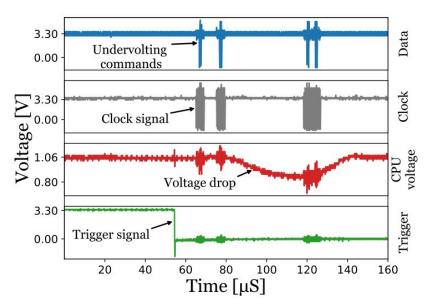


# VoltPillager: Hardware undervolting



## VoltPillager: Glitch Parameters





# Let's Inject Some Fault

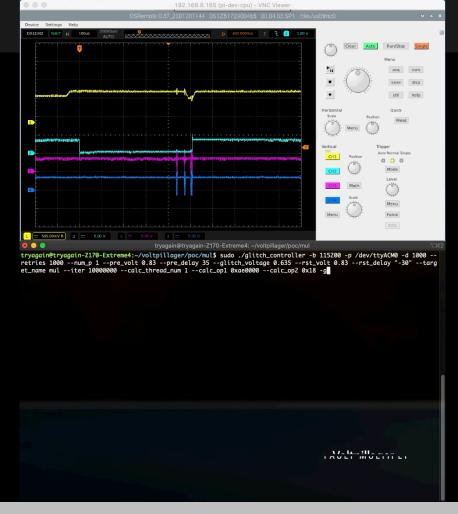
### Library for undervolting

```
// configure the glitch
// Z170 2GHz
configure_glitch_with_delay(1,0.83, 35, 0.63, -30, 0.83, 100);
// Target ecall
flag1++;
asm volatile("" ::: "memory");
    // TRIGGER
    TRIGGER SET
    sgx_ret = rsa_dec_ecall(eid, &res_var, buffer, iterations);
    if (SGX_SUCCESS != sgx_ret){
            printf("[ERROR]: sgx error 0x%x\n", sgx_ret);
asm volatile("" ::: "memory");
flag1++;
 / RESET TRIGGER
    TRIGGER_RST
```

## Fault Injection with VoltPillager

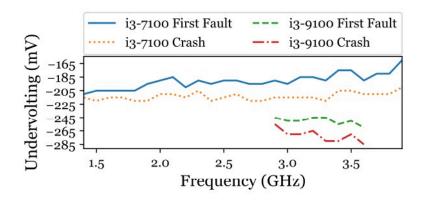
- Multiplication Fault
- RSA Fault (in SGX)
- AES-NI Fault (in SGX)
  - mbedtls aesni
  - Open Enclave file-encryptor
- Delayed-Write Fault

# Multiplication

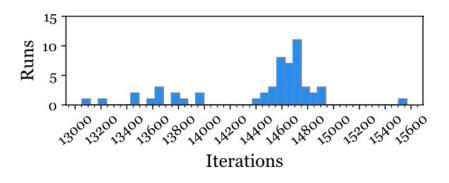


Hardware Based CPU Undervolting on The Cheap -- Stealing Your Secrets for \$30

## VoltPillager V.S. Plundervolt



**4VID Steps** 

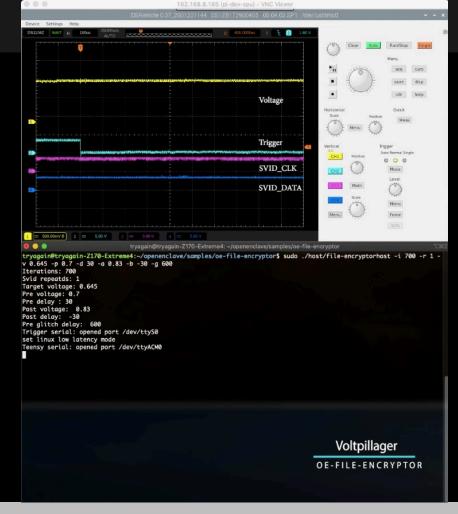


14,634 ± 300 -> 75% of faults

# Fault Encryptions

### Fault Encryptions

- sgx\_crt\_rsa PoC of Plundervolt
  - Recover the private the key
- sgx\_aes\_ni
- Open Enclave file-encryptor sample (AES-CBC)



Hardware Based CPU Undervolting on The Cheap -- Stealing Your Secrets for \$30

# Delayed-write fault

#### Delayed-Write Fault – Initial PoC

```
Should never happen
                                                                 -0x18(%rbp),%eax
                                                         1 mov
5 do {
                                                         2// compare operand1 (%eax) and operand2
    if(operand1 != operand2)
                                                                 -0x14(\%rbp), %eax
         faulty = 1;
                                                         4// continue at no_fault if equal
                                                                 no fault
   operand1++;
                                                         6 // else set faulty = 1
    operand2++;
                                                                 $0x1,0x20290f(%rip)
   i++;
                                                         8 // Increment operands and counter
   while(faulty == 0 && i < iterations);</pre>
                                                         13 // ... trigger code and fault check omitted ...
                                                        10 addl
                                                                $0x1.-0x14(%rbp)
                                                        11 addl
                                                                 $0x1,-0x1c(%rbp)
```

Not committed when CMP happen

Observed using VoltPillager

#### Delayed-Write Fault – Practical Exploitation

```
l uint32_t array[8] = { 0 };
2 // Attacker-supplied out-of-bounds size

int copy_size = 7;

// Ensure we stay within bounds

if(copy_size >= 5)

copy_size = 4;

// overwrite elements 4, 3, 2, 1

while(copy_size >= 1) {

array[copy_size] = 0xabababab;

copy_size --;
}
```

#### Normal execution:

	00	AB	AB	АВ	AB	00	00	00
--	----	----	----	----	----	----	----	----

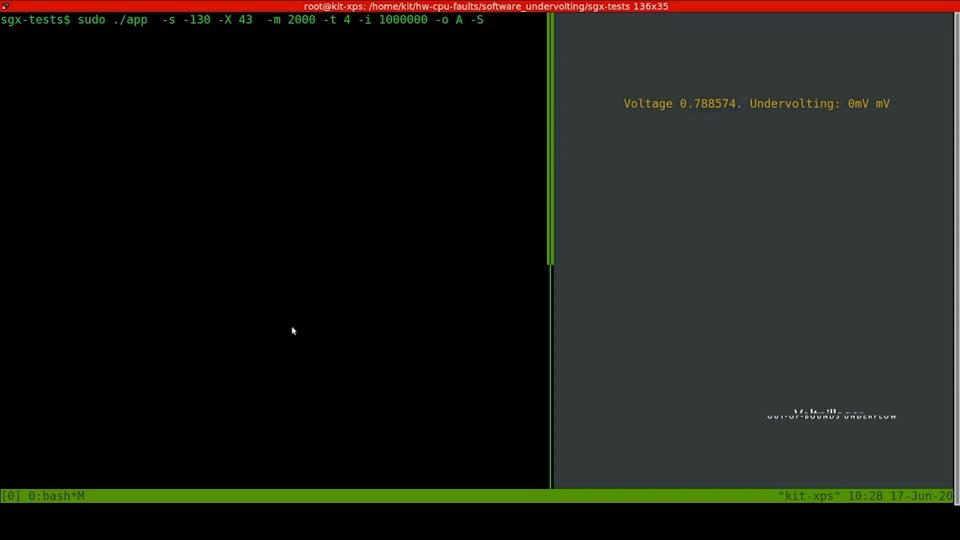
#### Fault 1 causing out-of-bounds underflow:

<b>AB</b>   AB   AB   AB   00   00.	. 00
-------------------------------------	------

#### Fault 2 causing out-of-bounds overflow:

		00	AB	АВ	AB	AB	AB	AB	AB
--	--	----	----	----	----	----	----	----	----



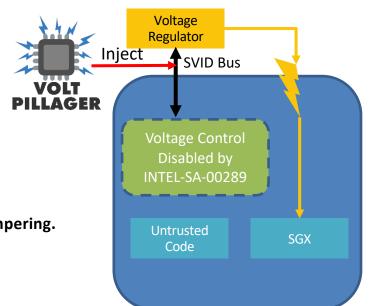


# Intel's response

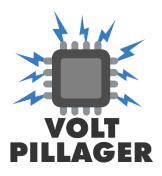
#### Intel's Response

"... opening the case and tampering of internal hardware to compromise SGX is out of scope for SGX threat model. Patches for CVE-2019-11157 (Plundervolt) were not designed to protect against hardware-based attacks as per the threat model" - Intel

But.....A lot of developers still think SGX can protect against hardware tempering.



# Summary



- 1st hardware based undervolting against Intel CPUs
- Physical access -> CVE- 2019-11157(Plundervolt)
- Build for \$30
- Rethink of Intel SGX Threat Model

# Thank you.



https://zt-chen.github.io/voltpillager/