On-hardware debugging of IP cores with free tools

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Who am I...

- not really a software developer
  ...but write code sometimes
- developing embedded systems for 25 years
- VME, CompactPCI, AdvancedTCA, SoM
- FPGA and SoC-FPGA (Altera/Intel, Microsemi/Microchip)
- VHDL (RTL-code, no, it is not a software)

My usual problem with the software is how to make it run on a hardware which is known not to be working yet and how to bring-up and test this hardware. With a soft-core CPU it is getting even worse.

Why software develpers should care about FPGA

- conventional hardware architectures are stuck
- the only two mainstream HDLs represent software technology level of a stone age (well, last century)

Therefore...

- you need it to make next generation software run on heterogeneous and malleable hardware
- industry needs your help to move forward

Free software for HDL developers

Simulate it!!

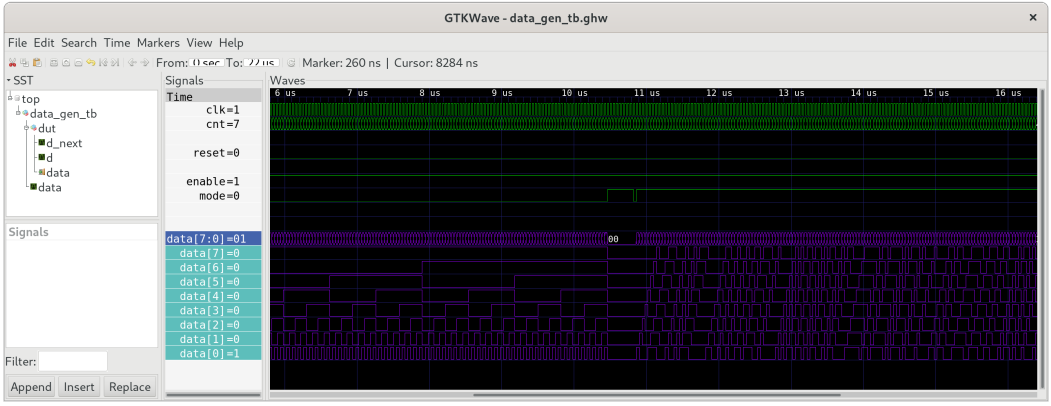
- Verilog HDL
  - Verilator (`https://www.veripool.org/wiki/verilator`)
  - Icarus Verilog (`http://iverilog.icarus.com/`)
  - Yosys (`http://www.clifford.at/yosys/`)
- VHDL: `ghdl` (`http://ghdl.free.fr/`)
  GHDL is an open-source simulator for the VHDL language.
- GTKWave (`http://gtkwave.sourceforge.net/`)
  GTKWave is a fully featured cross-platform wave viewer

Unit and regression testing for hardware blocks (Python cocotb, VPI, etc.)

VHDL code snippet

```
process (d, mode)
begin
  if mode = '0' then
    d_next <= std_logic_vector(unsigned(d) + 1);
  else
    d_next(7 downto 1) <= d(6 downto 0);
    d_next(0) <= d(7) xor d(5) xor d(4) xor d(3);
  end if;
end process;
```

GTKWave with GHDL simulation results



. . . and live demo

On-chip instrumentation

Proprietary and vendor specific tools (and their problems)

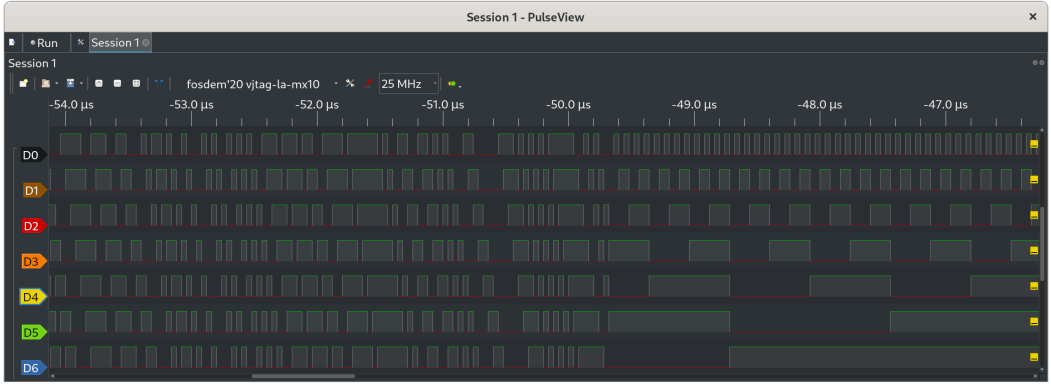
- Altera/Intel SignalTAP
- Xilinx ChipScope
- Synopsys Identify RTL Debugger
- Microsemi/Microchip SmartDebug

What is in common: standard inteface to the hardware IEEE 1149.1 (JTAG)

Assembling a puzzle

- Free software to speak with hardware on IEEE-1149.1
  - UrJTAG (`http://urjtag.org/`)
  - OpenOCD (`http://openocd.org/`)
- libsigrok (`https://sigrok.org/`)
- PulseView (sigrok Logic Analyzer GUI)
- SpiderBoard with SpiderSoM (`http://www.spiderboard.org/`)
  or MX10 (`https://www.aries-embedded.com/system-on-module/fpga/`)
  Altera/Intel MAX10 FPGA module with built-in USB-to-JTAG interface

Logic Analyzer trace



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Challenges ahead

- **integration**
- support for different hardware interfaces, FPGA vendors, device families
- automated design instrumentation (kudos to vendor tools)
- IEEE-1149.7, IEEE-1687 (2014), etc.
- integration with software debugging tools

Thank you!

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Questions?..