

Reimagining EDSAC in Open Source

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Overview









Predecessors





Building EDSAC





EDSAC





EDSAC's Memory





EDSAC Architecture



A Tutorial Guide to the EDSAC Simulator, Department of Computer Science, University of Warwick

EDSAC Data





A Tutorial Guide to the EDSAC Simulator, Department of Computer Science, University of Warwick

EDSAC Instructions



A *n* Add value at storage location *n* to the accumulator

- S n Subtract value at storage location n from the accumulator
- ...
- Y Round the accumulator to 34 bits
- Z Stop the machine

Total of 18 instructions



A Tutorial Guide to the EDSAC Simulator, Department of Computer Science, University of Warwick

Program Input





Job Queue





Teleprinter





Bootstrap





EDSAC Initial Orders

6ESOTS2HSOT



Order bit pattern	Loc	Order	Meaning	Comment
00101 0 000000000 0 10101 0 0000000010 0 00101 0 00000000	0: 1: 2.	TOS H2S TOS	m[0]=A; ABC=0 R=m[2] m[0]=A; ABC=0	Put 10<<11 in R
00011 0 0000000110 0	3:	E6S	goto 6	Jump to main loop
00000 0 000000001 0	4:	P1S P5S	data 2 data 10	The constant 2
00000 0 0000000101 0	5.	105		
$00101 \ 0 \ 0000000000 \ 0$ $01000 \ 0 \ 0000000000 \ 0$	6: 7:	TOS	m[0]=A; ABC=0 m[0]=rdch()	Start of the main loop Get operation code
11100 0 000000000 0	8:	AOS	A += m[0]	Put it in A
00100 0 0000010000 0	9:	R16S	ABC>>=6	Shift and store it
00101 0 0000000000 1	10:	TOL	w[0]=AB; ABC=0	so that it becomes the senior 5 bits of $m[0]$ m[1] is now zero
01000 0 000000010 0	11:	I2S	m[2]=rdch()	Put next ch in $m[2]$
11100 0 000000010 0	12:	A2S	A+=m[2]	Put ch in A
01100 0 0000000101 0	13:	S5S	A = m[5]	A=ch-10
00011 0 0000010101 0	14:	E21S	if A>=0 goto 21	Jump to 21, if $ch \ge 10$
00101 0 0000000011 0	15:	T3S	m[3]=A; ABC=0	Clear A, $m[3]$ is junk
11111 0 000000001 0	16:	V1S	AB+=m[1]*R	A = m[1]*(10<<11)
11001 0 0000001000 0	17:	L8S	A<<=5	Shift 5 more places
	18:	A2S T1S	$A^{+=}m[2]$	Add the new digit
	20.	F115	m[1]-A; ABC=0	Repeat from 11
00011 0 0000001011 0	20.	LIIS	g000 11	
				A=2, it ch='S'(=12) A=15 if ch='L'(=25)
00100 0 000000100 0	21:	R4S	ABC>>=4	lenbit=0, if ch='S'
11100 0 000000001 0	22.	410	A	lenbit=1, if ch=`L'
11001 0 000000000 1	22:	A 15	A += m [1]	Shift to correct position
11100 0 000000000 0	23.	AOS	A += m [0]	Add in the operation field
00101 0 0000011111 0	25:	T31S	m[31] = A: ABC=0	Store the order
			[0-],	in next location
11100 0 0000011001 0	26:	A25S	A+=m[25]	Increment the address field of $m[25]$
11100 0 0000000100 0	27:	A4S	A = m[4]	m[4] holds 2
00111 0 0000011001 0	28:	U25S	m[25]=Å	Update m[25]
01100 0 0000011111 0	29:	S31S	A-=m[31]	Jump to 6, if there are
11011 0 0000000110 0	30:	G6S	if A <o 6<="" goto="" td=""><td>more orders to load</td></o>	more orders to load



EDSAC Initial Orders and Squares Program, Martin Richards, University of Cambridge Computer Laboratory

Wheeler Jumps

Location	Order	Notes		
p - 1	TOS	Move acc to loc 0 and zero acc		
p	ApS	Store current loc in acc	}	Main program
p + 1	EqS	Jump to loc q if acc positive	J	
	A3S Tq+rS	Loc 3 contains E2S, creates E <i>p</i> +2S Overwrite link order	}	Prologue
g + r - 1	TOS	Zero accumulator	٦	
q + r	E2S	Link order which will be modified	}	Epilogue



First Book on Programming

THE PREPARATION OF PROGRAMS FOR AN ELECTRONIC DIGITAL COMPUTER

> With special reference to the EDSAC and the use of a library of subroutines

> > 63

MAURICE V. WILKES Director of the Mathematical Laboratory of the University of Cambridge

DAVID J. WHEELER

and Stanley Gill





Famous Programs

 $180(2^{127}-1)^2+1$

Gene		Gene		Gene		
percentage	Deviate	percentage	Deviate	percentage	Deviate	
50	.00000	20.0	.64827	5.0	1.30643	
49	.01908	19.5	.66247	4.8	1.32331	
48	.03817	19.0	.67691	4.6	1.34080	
47	.05729	18.5	.69161	4.4	1.35896	
46	.07645	18.0	.70658	4.2	1.37784	
45	.09566	17.5	.72184	4.0	1.39752	
44	.11493	17.0	.73740	3.8	1.41807	
43	.13429	16.5	.75329	3.6	1.43958	
42	.15375	16.0	.76952	3.4	1,46216	
41	.17332	15.5	.78612	3.2	1.48594	
40	.19302	15.0	.80311	3.0	1.51106	
39	.21286	14.5	.82052	2.8	1.53771	
38	23286	14.0	.83837	2.6	1.56609	
37	.25304	13.5	.85669	2.4	1.59648	
36	.27341	13.0	.87553	2.2	1.62922	
35	.29400	12.5	.89492	2.0	1.66474	
34	.31483	12.0	.91492	1.8	1.70360	
33	.33592	11.5	.93556	1.6	1.74656	
32	.35729	11.0	.95691	1.4	1.79468	
31	.37897	10.5	.97902	1.2	1.84951	
30	. 40099	10.0	1.00198	1.0	1.91340	
29	.42338	9.5	1.02586	0.9	1.94988	
28	.44617	9.0	1.05076	0.8	1.99029	
27	.46940	8.5	1.07680	0.7	2.03565	
26	.49311	8.0	1.10411	0.6	2.08745	
25	.51734	7.5	1.13285	0.5	2.14795	
24	.54214	7.0	1.16321	0.4	2.22095	
23	.56757	6.5	1.19543	0.3	2.31345	
22	.59369	6.0	1.22978	0.2	2.44101	
21	.62056	5.5	1.26662	0.1	2.65223	







Popular Appreciation

The "brain" [computer] may one day come down to our level [of the common people] and help with our income-tax and book-keeping calculations. But this is speculation and there is no sign of it so far.



Reimagined EDSAC



Field Programmable Gate Array (FPGA)









EDSAC Verilog







Reimagined Paper Tape





Reimagined Paper Tape Reader







Paper Tape Reader Output





Raw Sensor Data





Sprocket Hole





 $slope = \frac{\mathrm{d}x}{\mathrm{d}t}$











Exponential Smoothing



1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64



Exponential Smoothing



1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64



Exponential Smoothing



1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64



Deltas



















Data Bit 2





Data Bit 2





Data Bit 2





Paper Tape Reader Output





Paper Tape Reader Demo

	/dev/ttyUSB0	. ¤ ×
		Send
Get ready		
Go		
TOS		
H2S		
TOS		
E6S		
P1S		
P5S		
TOS		
105		
A0S		
R16S		
TOL		
I2S		
A2S		
S5S		
Autoscroll	No line ending 🛛 👻	115200 baud 💌



Mercury Delay Line





























Reimagined Delay Line













"The Actual Solution"



Microphone Circuit





Microphone Circuit





Testing the Microphone Circuit





Speaker Circuit





Air Delay Line Demo





Chip Hack



Summary





Thank You





Contact

- Make your own EDSAC peripherals:
 - github.com/embecosm/edsac-peripherals
- Hatim Kanchwala Verilog EDSAC:
 - github.com/librecores/gsoc-museum-edsac
- Chip Hack repository:
 - github.com/embecosm/chiphack
- More information on the myStorm:
 - mystorm.uk





Questions?

www.embecosm.com



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