

# LibrePCB

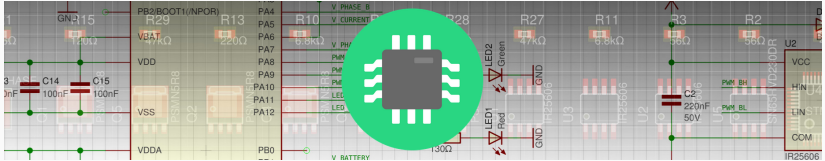
A new, powerful and intuitive EDA tool for everyone

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Urban Bruhin

February 3, 2018

# About LibrePCB



## Free/OpenSource EDA Suite

- Multiplatform   
- Written from scratch in C++11/Qt5
- Development started in 2013
- Website: <http://librepcb.org/>
- GitHub: <https://github.com/LibrePCB/LibrePCB>

## Frustration about existing EDA tools

- Library system
- File format
- Usability

## Problem

- Different library types (e.g. \*.lib, \*.pretty, \*.3dshapes)
- Tools do not (completely) handle library management
  - No integrated tool to install and update libraries
  - No dependency management
  - Complicated project library management

## Problem

- Different library types (e.g. \*.lib, \*.pretty, \*.3dshapes)
- Tools do not (completely) handle library management
  - No integrated tool to install and update libraries
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  - Complicated project library management

## Result

- It's up to the user to manage his libraries (which is a pain)

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## Libraries

Access the largest collection of free and open source component libraries.

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### si5317\_10.lbr by samuell

Si5317 jitter filter from Silicon Labs. This is a filter specially designed for clock signals. The Si5317 is fully configurable, allowing both the work frequency and loop bandwidth to be set. It admits different types of clocks (CML, CMOS, LVDS or LVPECL), being capable of producing such levels too. Based on Silicon Laboratories' 3rd-generation DSPLL technology, the Si5317 outputs a clock signal having a typical jitter of 300fs.

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### sxx8xsx\_10.lbr by samuell

Sxx8xsx SCRs (silicon controlled rectifiers) from Littelfuse (Teccor). These thyristors can control currents up to 0.51A (or 0.8A average), having a maximum voltage drop of 1.7V.


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### polyfuse-smd\_20.lbr by samuell

Littelfuse Polyfuse devices. This new version of the library contains the most recent surface mount

# Library Management

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Project '/home/user/test/test.pro'

## Libraries

Access the largest collection of libraries

Search for Libraries

**si5317\_10.lbr** by si5317

Si5317 jitter filter from Silicon Laboratories, fully configurable, all types of clocks (CML, CMOS), typical jitter of 300fs.

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**sxx8xsx\_10.lbr** by sxx8xsx

Sxx8xsx SCRs (silicon controlled rectifiers) currents up to 0.51A

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**polyfuse-smd\_20.lbr** by Littelfuse

Littelfuse Polyfuse device

### Component library files

- power
- device
- transistors
- conn
- linear
- regul
- 74xx
- cmos4000
- adc-dac
- memory
- xilinx

[Add](#) [Insert](#) [Remove](#) [Up](#) [Down](#)

### User defined search path

[Add](#) [Insert](#) [Remove](#)

### Current search path list

- /home/user/test
- /snap/kicad-snap/2/usr/share/kicad/library
- /snap/kicad-snap/2/usr/share/kicad/template
- /usr/local/share

☒ Check for cache/library conflicts when loading schematic

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# Library Management



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Littelfuse Polyfuse de

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User defined search path

Current search path list

/home/user/test  
/snap/kicad-snap/2/usr/s  
/snap/kicad-snap/2/usr/s  
/usr/local/share

☒ Check for cache/library conflicts when loading schematic

Cancel

OK

## PCB Library Tables

Library Tables by Scope

Table: /home/user/snap/kicad-snap/common/.config/kicad/fp-lib-table

	Nickname	Library Path
15	Connectors_JAE	\$(KISYSMOD)/Connectors_JAE.pretty
16	Connectors_JST	\$(KISYSMOD)/Connectors_JST.pretty
17	Connectors_Molex	\$(KISYSMOD)/Connectors_Molex.pretty
18	Connectors_Multicomp	\$(KISYSMOD)/Connectors_Multicomp.pretty

Global Libraries

Project Specific Libraries

Append with Wizard

Append Library

Remove Library

Move Up

Move Down

Path Substitutions


	Environment Variable	Path Segment
1	KIPRJMOD	/home/user/test
2	KISYS3DMOD	\$\$SNAP/usr/share/kicad/modules/packages3d/
3	KISYSMOD	\$\$SNAP/usr/share/kicad/modules/

Cancel

OK



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Si5317 jitter filter from Silicon Labs, fully configurable, all types of clocks (CML, CMOS), typical jitter of 300fs.  

Download Like

sxx8xsx\_10.lbr by Silicon Labs  
Sxx8xsx SxRs (silicon) currents up to 0.51A (typical).  

Download Like

polyfuse-smd\_20.lbr by Littelfuse  
Littelfuse Polyfuse device.  

Download Like

Component library files

power

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/home/user/test

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/snap/kicad-snap/2/usr/share

/usr/local/share

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Cancel

OK

PCB Library Tables

Library Tables by Scope

Table: /home/user/snap/kicad-snap/common/.config/kicad/fp-lib-table

Symbol Name	Library Path
Connectors_JST.pretty	\$(KISYSMOD)/Connectors_JST.pretty
Connectors_Molex.pretty	\$(KISYSMOD)/Connectors_Molex.pretty
Connectors_Multicomp.pretty	\$(KISYSMOD)/Connectors_Multicomp.pretty

Global Libraries

Project Specific Libraries

Append Wizard

Append Library

Remove Library

Move Up

Move Down

Path Segment

Symbol Variable	Path Segment
1 KIPROMOD	/home/user/test
2 KISYS3DMOD	\$(SNAP)/usr/share/kicad/modules/packages3d/
3 KISYSMOD	\$(SNAP)/usr/share/kicad/modules/

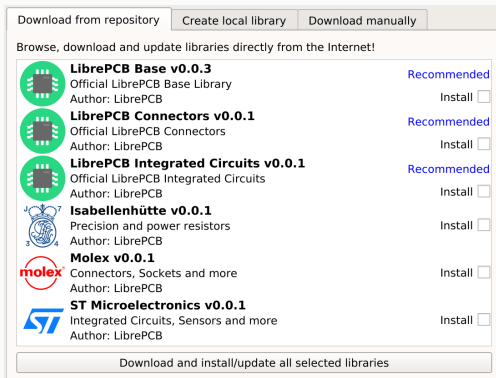
Cancel

OK

3/16

## Solution

- Integrated library manager with dependency management
- Libraries can contain any entity type (symbols, footprint, ...)
- The application handles basically **everything** for you



## Problem

- Everything is referenced by name
- References across libraries not possible in some tools

# Library References

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## Result

- Broken references after changing names
- Name conflicts because they are not unique
- Many duplicates accross different libraries

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## Solution


- Every entity is identified by a random UUID
- References always by UUID, never by name
- Entities can be referenced across different libraries

## Library References


```
(librepcb_symbol
 (uuid f0061936-5169-49c9-bfa5-4efc8108cd1c)
 (name "Connector 1x4")
 ...
 (pin 169d6728-7108-4600-aa48-765711db01bc (name "1")
 (pos -20.32 40.64) (rot 0.0) (length 5.08)
 )
 (pin 1c49822e-fd83-452a-a7a6-f4ae1357a0c7 (name "2")
 (pos 20.32 -40.64) (rot 180.0) (length 5.08)
 )
 (pin 208bd2b9-ed07-4df5-b5ab-a89fb03378d5 (name "3")
 (pos 20.32 -38.1) (rot 180.0) (length 5.08)
 )
 (pin 2684075c-566e-43fb-b025-17cf43badaf4 (name "4")
 (pos 20.32 -12.7) (rot 180.0) (length 5.08)
 )
 )
 )
```

## Problem

- Impossible to have different symbols for the same component

e.g. Resistor: 

## Problem

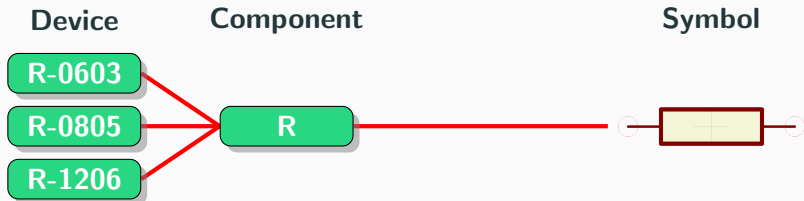
- Impossible to have different symbols for the same component  
e.g. Resistor: 

## Result

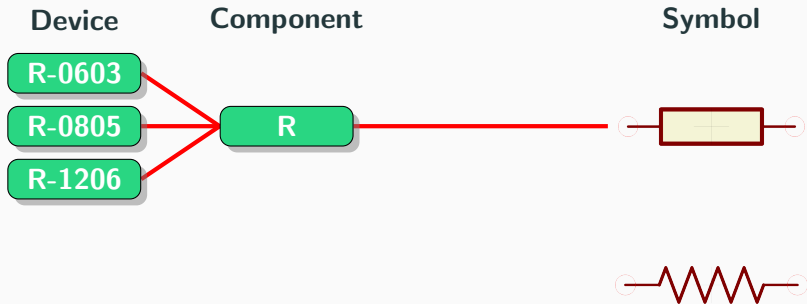
- Duplicate components (same functionality, different symbol)



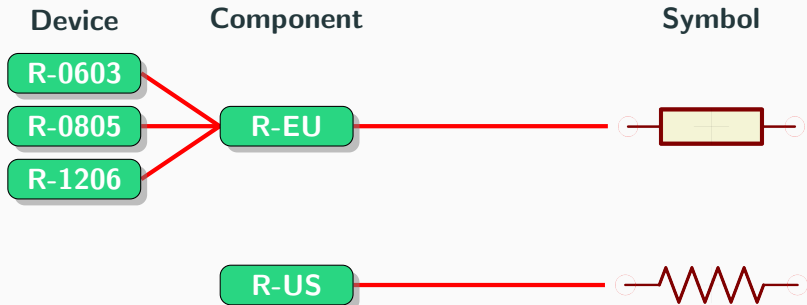
# Symbol Variants



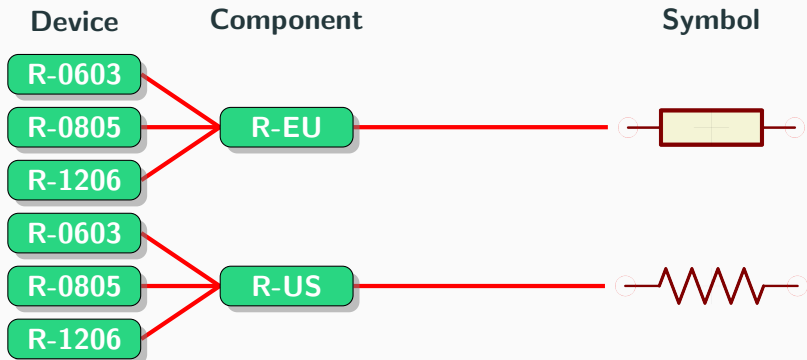
# Symbol Variants



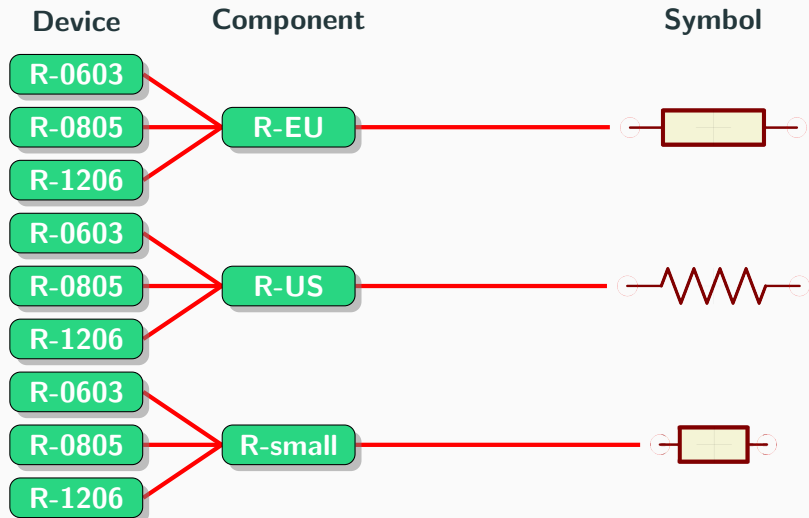
# Symbol Variants



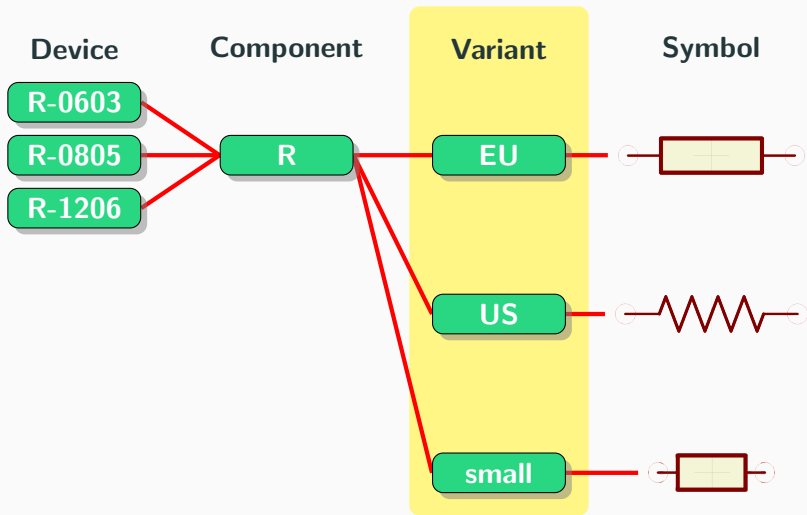
# Symbol Variants



# Symbol Variants



# Symbol Variants



# Footprint Variants

## Problem

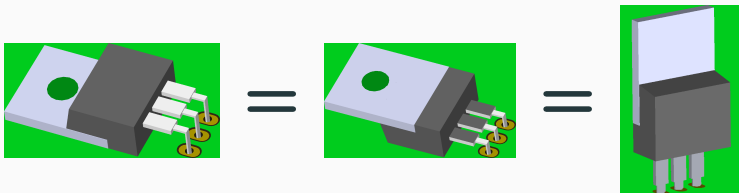
- Libraries do not provide an abstraction layer for **packages**



# Footprint Variants

## Problem

- Libraries do not provide an abstraction layer for **packages**



## Result

- Devices need to know every footprint variant of their package



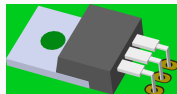
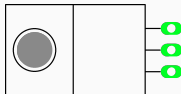
# Footprint Variants

Device

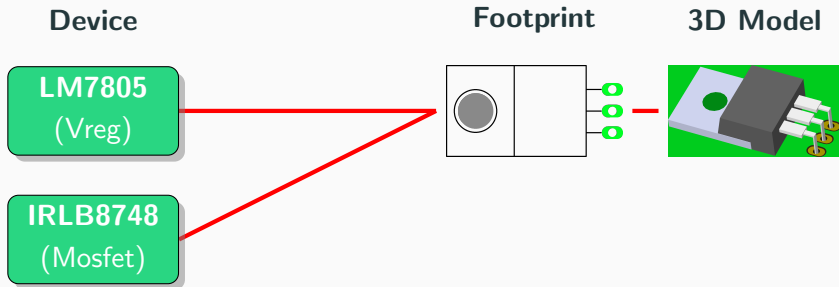
Footprint

3D Model

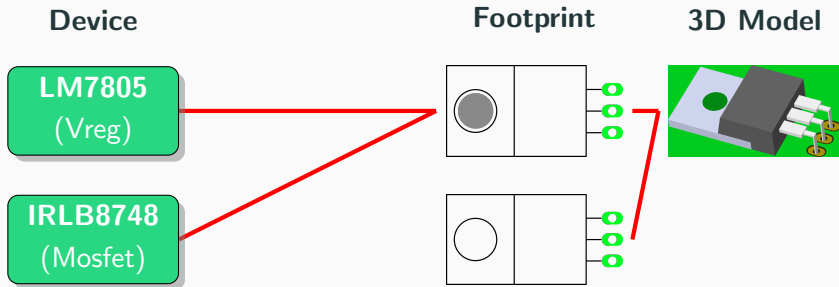
LM7805  
(Vreg)



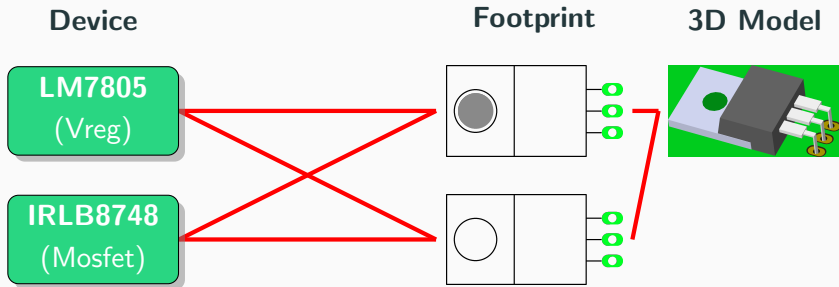
# Footprint Variants



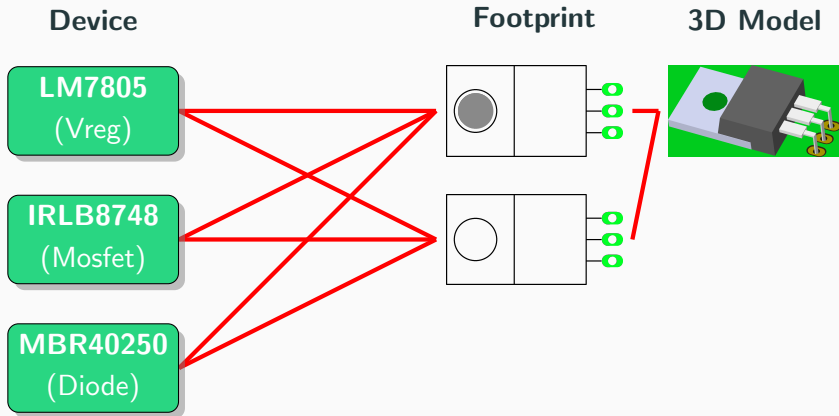
# Footprint Variants



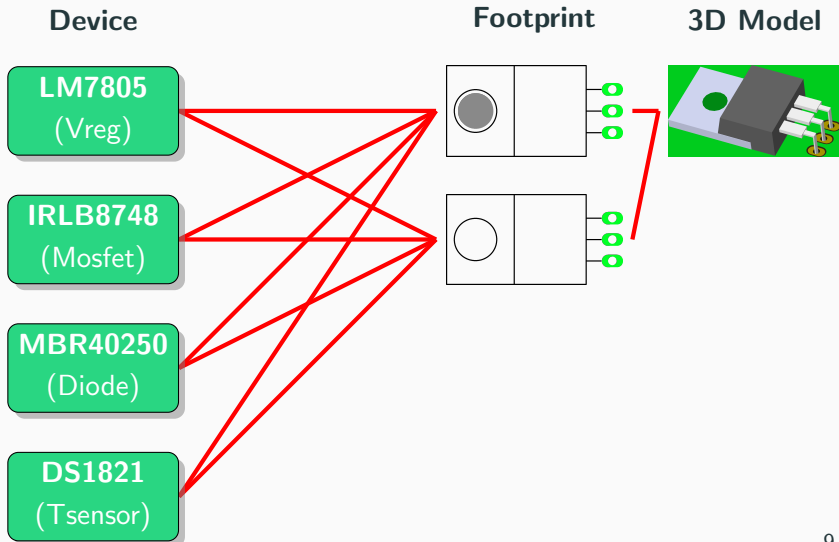
# Footprint Variants



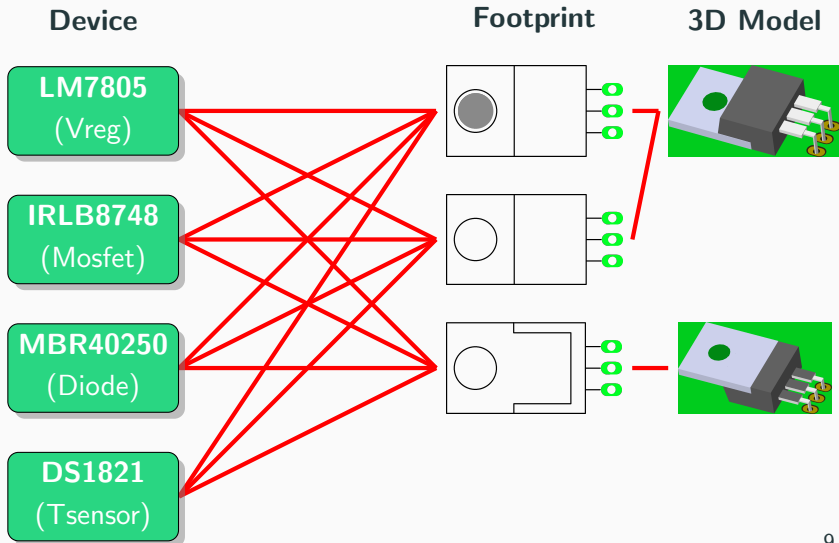
# Footprint Variants



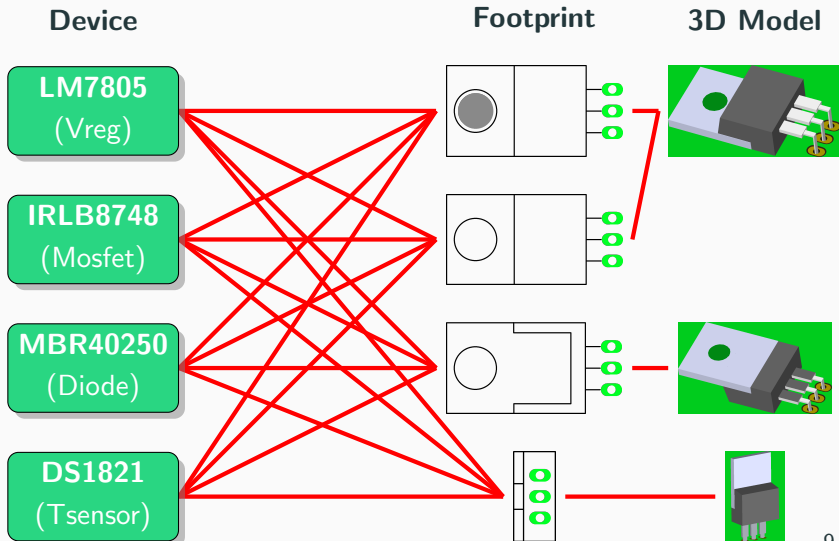
# Footprint Variants



# Footprint Variants

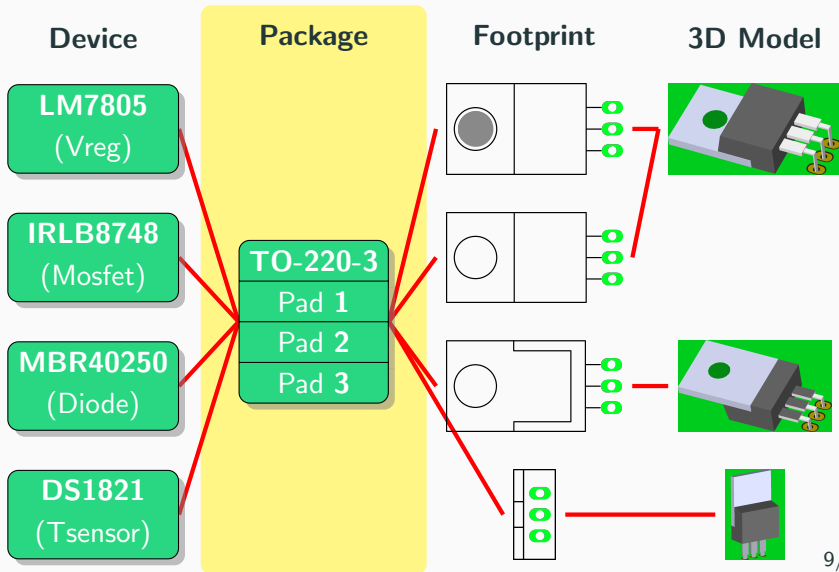


# Footprint Variants





# Footprint Variants



## Problem

- Important and unimportant data mixed
- Unclear which files to version control

# Version Control Systems

## Problem

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## Result

- Local changes even if nothing modified
- Very large and opaque diffs/commits
- Merging is basically impossible

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## Problem

- Important and unimportant data mixed
- Unclear which files to version control

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- Local changes even if nothing modified
- Very large and opaque diffs/commits
- Merging is basically impossible

## Solution

- Many small files for higher granularity
- Unimportant data strictly separated
- Automatic creation of .gitignore

```
MyProject
├── .gitignore
├── boards
│   ├── default.lp
├── core
│   ├── circuit.lp
│   ├── erc.lp
│   └── settings.lp
├── output
│   └── ...
├── schematics
│   ├── power.lp
│   └── logic.lp
├── user
│   └── ...
```

# Version Control Systems

```
--- a/test.kicad_pcb
+++ b/test.kicad_pcb
@@ -3,7 +3,7 @@
    (general
      (no_connects 0)
-     (area 41.834999 87.554999 233.755001 153.745001)
+     (area 20.171999 28.969758 233.755001 157.374234)
      (drawings 4)
@@ -21,7 +21,7 @@
      (36 B.SilkS user)
-     (37 F.SilkS user)
+     (37 F.SilkS user hide)
      (38 B.Mask user hide)
@@ -62,7 +62,7 @@
      (aux_axis_origin 0 0)
-     (visible_elements FFFC4601)
+     (visible_elements FFFC4609)
      (pcbplotparams
```

## Problem

- Files are **not really** human readable

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## Result

- Diffs are very hard to understand
- Limited use of version control systems

# Version Control Systems

## Problem

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- Diffs are very hard to understand
- Limited use of version control systems

## Solution







- Don't just consider text-based file formats as human readable!
- Control every tiny detail of the generated files
- Consider opaque parts of files as bugs and fix them



# Project Status

Library Management		
Library Editor		
Schematic Editor		(except missing copy&paste)
Board Editor		(no planes, airwires, DRC, ...)
Export (e.g. Gerber)		
Available Libraries		

# Project Status

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Board Editor		(no planes, airwires, DRC, ...)
Export (e.g. Gerber)		
Available Libraries		



- File format not yet considered as stable!
- Breaking changes can (and will) occur!

## Nightly builds available for download

- Applmage for Linux
- ZIP with \*.exe for Windows

## Documentation

[https://docs.librepcb.org/getting\\_started/](https://docs.librepcb.org/getting_started/)

**Demo Time!**

## Priority 1: First stable release

- Stabilize file format (last breaking changes)
- Make board editor usable (planes, airwires, fonts, DRC)
- Prepare first stable release (fix bugs, polish GUI, ...)

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## Priority 2: Add more functionality

- Clipboard ✂️ 📄 📄
- Hierarchical sheets
- 3D board viewer
- ...

# Contributors welcome!

<https://github.com/LibrePCB/LibrePCB/blob/master/CONTRIBUTING.md>

- Participate in issues
  - Open pull requests
- Improve documentation
- Donate (Patreon or Bitcoin)

# Thank you!

<http://librepcb.org>