QUCS
Quite Universal Circuit Simulator

Overview and Status

Guilherme Brondani Torri

FOSDEM 2017
EDA Developer room
Brussels, 04 February 2016

Qucs /kju:ks/

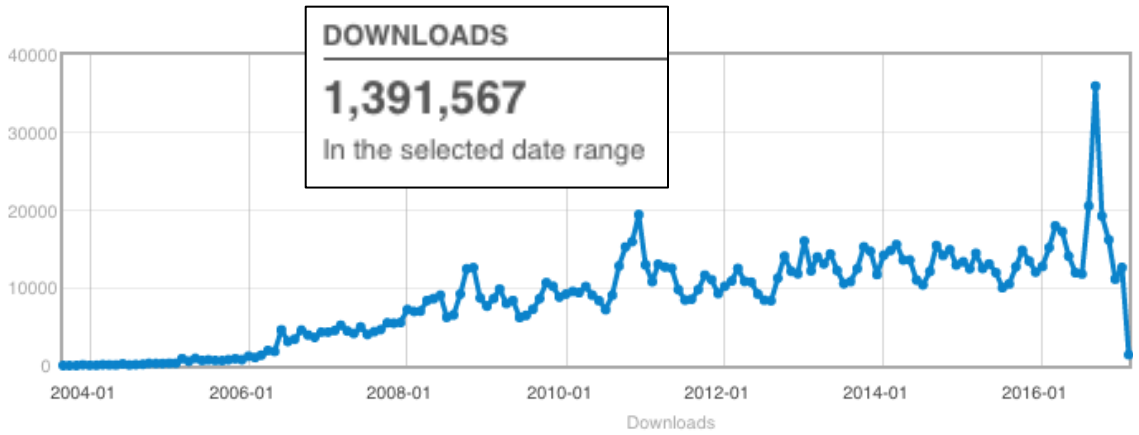
- Overview
  - Project background
  - Features
- Status
  - Development
  - Next release
- Final Remarks

Project background

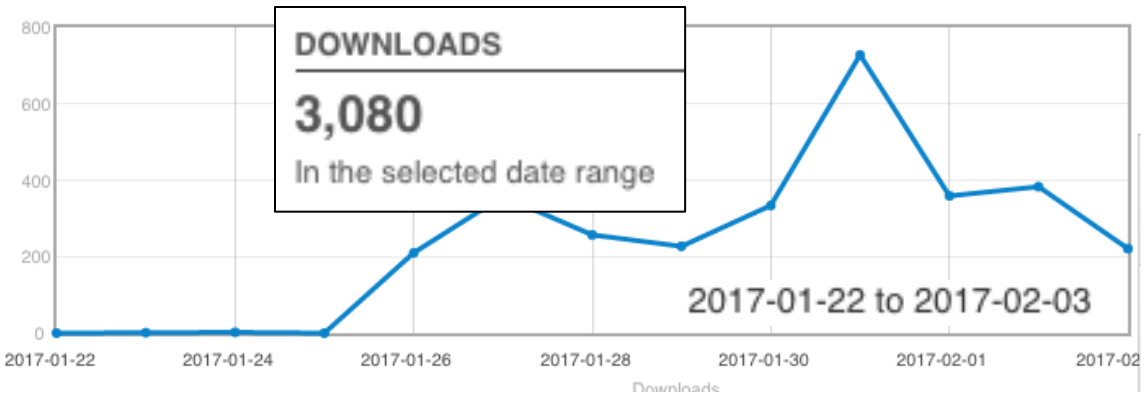
- Created at TU-Berlin
  - Michael Margraf
  - Stefan Jahn
- GPLv2+
- 20+ contributors
- 20 languages
- Cross-platform
- Users
  - Education
  - Research
  - Hobbyists
  - Industry

Website counter
1460126
visitors since 2005/04/27

- 2003 to 2017



- Qucs 0.0.19 - Windows



Main Features

- Schematic capture
- Simulator

- Data visualization
- Equation system
- Component library
- Design / synthesis tools

- Modeling tools
  - Spice converter (limited)
  - Equation defined device (EDD)
  - Verilog-A model builder
- Post-processing
  - Octave/MATLAB
  - Python
- Dependencies
  - C++ compiler
  - Qt4 (with Qt3Support)
  - Autotools / CMake
  - gperf / flex / bison
  - ADMS
  - LaTex

Experimental

- Qucs-S
  - SPICE support
  - Ngspice, Xyce, SpiceOpus
  - Verilog-A generators
  - XSPICE generators
  - …

https://ra3xdh.github.io/

- Gnucsator
  - gnucap based qucsator implementation

https://github.com/Qucs/gnucsator

- QUCS →gschem

https://github.com/erichVK5/translate2geda/

Support

- Website

http://qucs.sourceforge.net

- Active maintainers:
  - Guilherme Brondani Torri
  - Claudio Girardi
  - Vadim Kuznetsov
  - Felix Salfelder
  - Andrés Martínez Mera
  - Mike Brinson

- Documentation
  - Help
  - Tutorial Workbook
  - Report Workbook
  - Technical Manual

- SourceForge
  - Binaries
  - Git repository (mirror)
  - Issue tracker
  - Forum / mailing lists

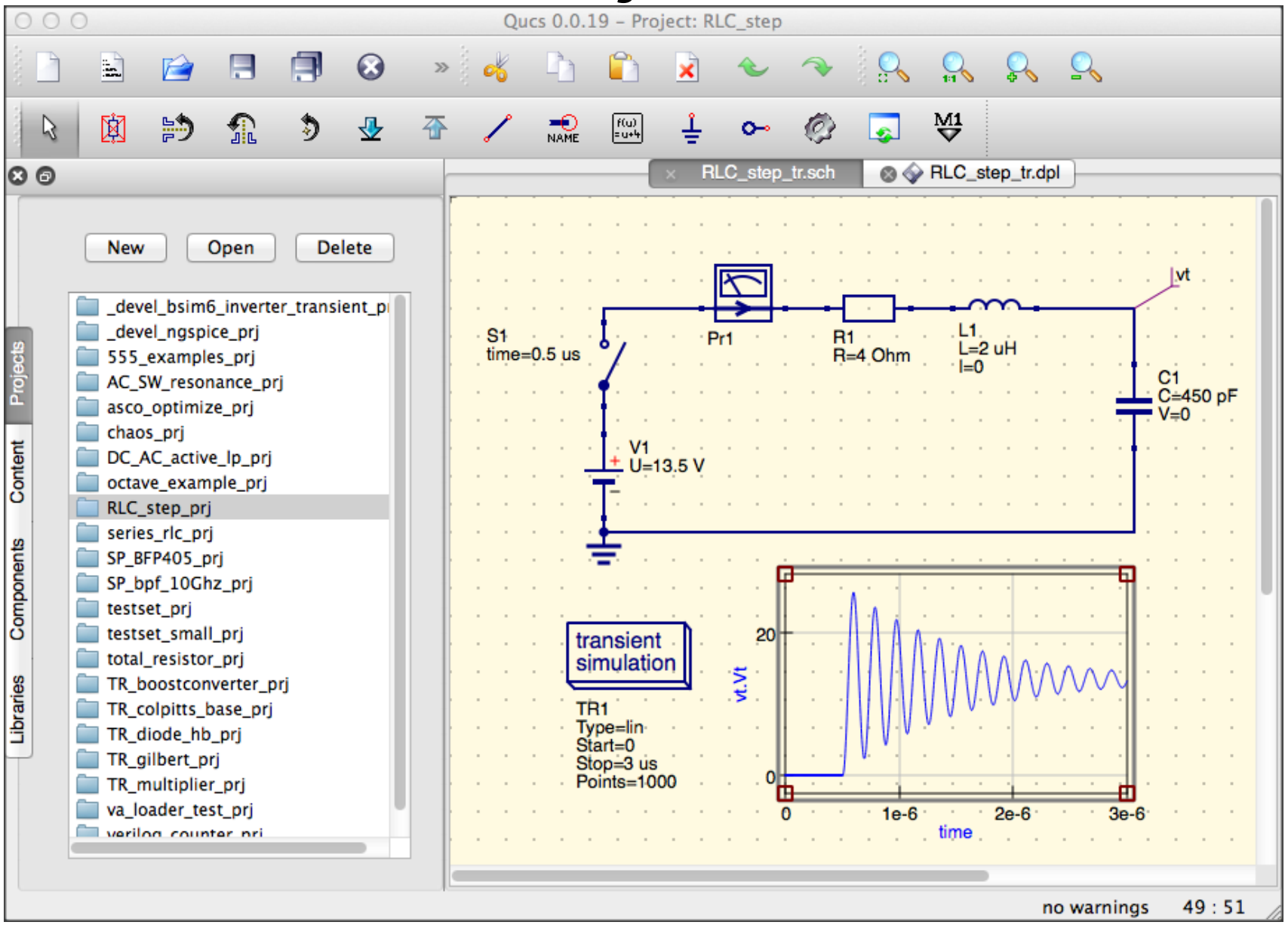
- GitHub
  - Git repository (preferred)
  - Issue tracker
  - Wiki
  - Travis CI
  - AppVeyor

Tools

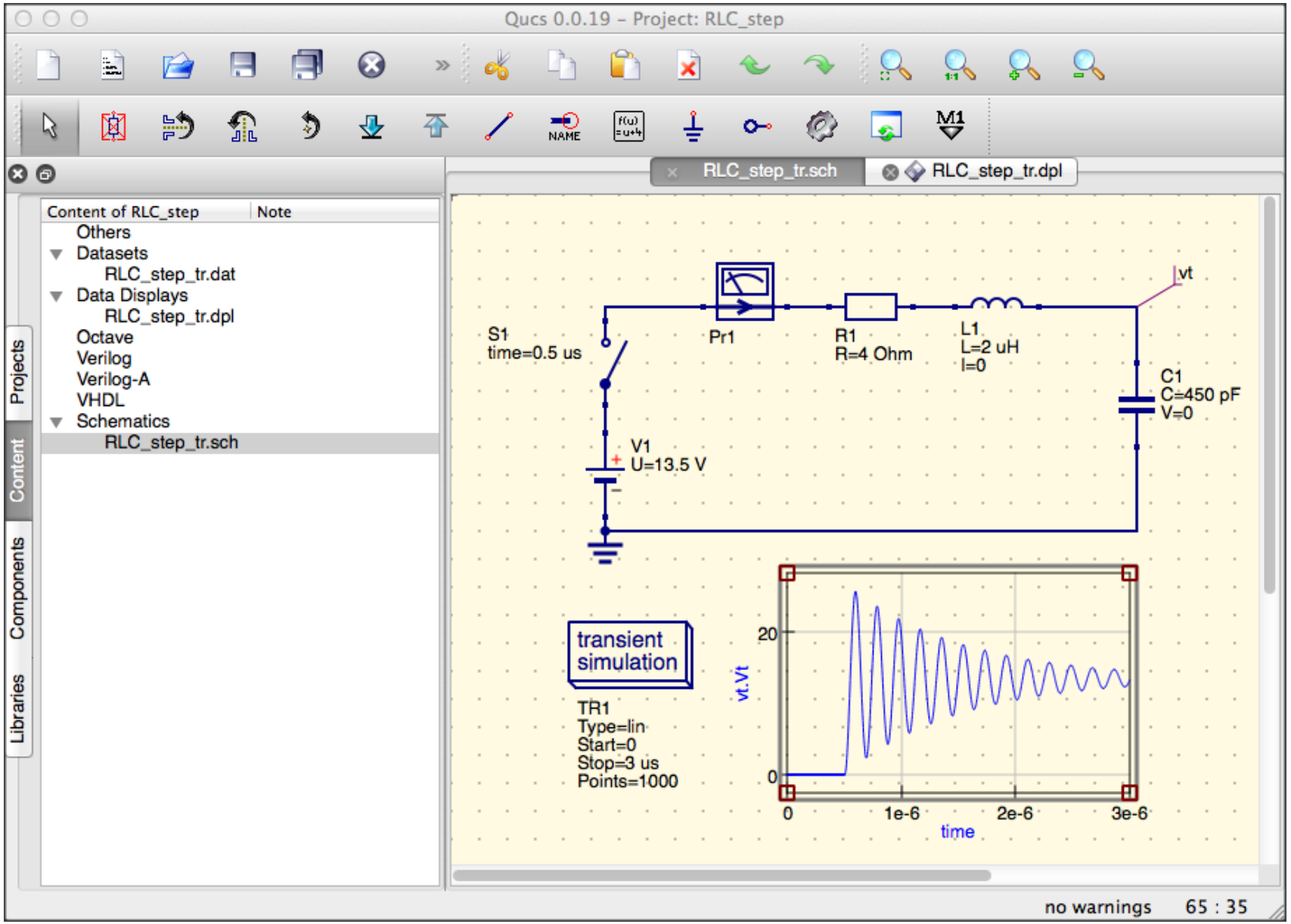
- Graphical Interface
  - Qucs
  - ActiveFilter
  - Attenuator
  - Editor
  - Filter
  - Help
  - Matching
  - Library
  - Rescodes
  - Transcalc
- ~ 170 components

- Command Line
  - qucs
  - qucsator
  - qucsconv
- Third-party and scripts
  - asco
  - admsXml
  - iverilog
  - freehdl
  - ps2sp
  - octave
  - python

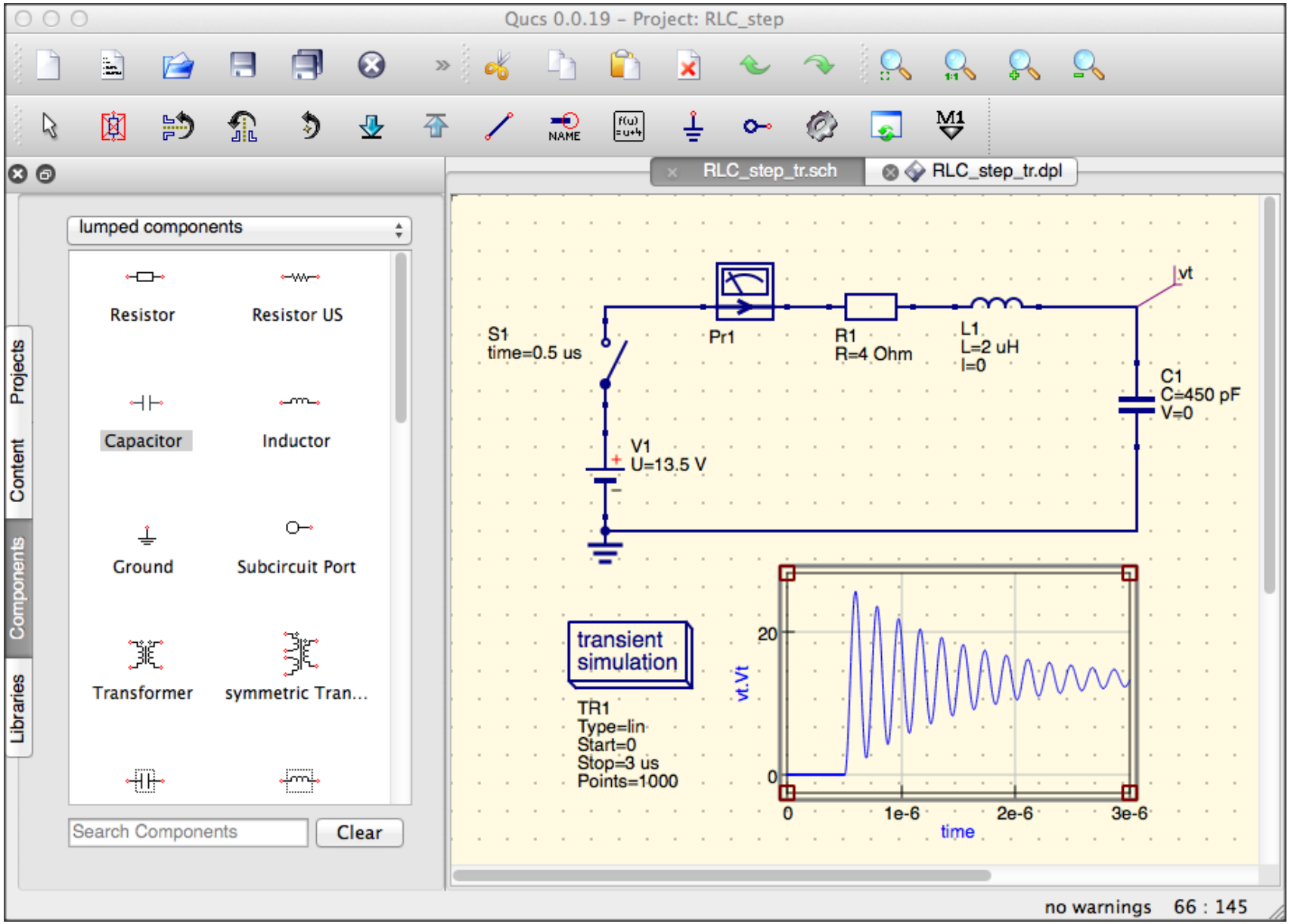
Projects


Qucs 0.0.19 – Project: RLC_step
RLC_step_tr.sch
RLC_step_tr.dpl
New
Open
Delete
Projects
Content
Components
Libraries
_devel_bsim6_inverter_transient_pr
_devel_ngspice_prj
555_examples_prj
AC_SW_resonance_prj
asco_optimize_prj
chaos_prj
DC_AC_active_lp_prj
octave_example_prj
RLC_step_prj
series_rlc_prj
SP_BFP405_prj
SP_bpf_10Ghz_prj
testset_prj
testset_small_prj
total_resistor_prj
TR_boostconverter_prj
TR_colpitts_base_prj
TR_diode_hb_prj
TR_gilbert_prj
TR_multiplier_prj
va_loader_test_prj
S1
time=0.5 us
Pr1
R1
R=4 Ohm
L1
L=2 uH
I=0
vt
C1
C=450 pF
V=0
V1
U=13.5 V
transient
simulation
TR1
Type=lin
Start=0
Stop=3 us
Points=1000
vt.Vt
20
0
0
1e-6
2e-6
3e-6
time
no warnings
49 : 51

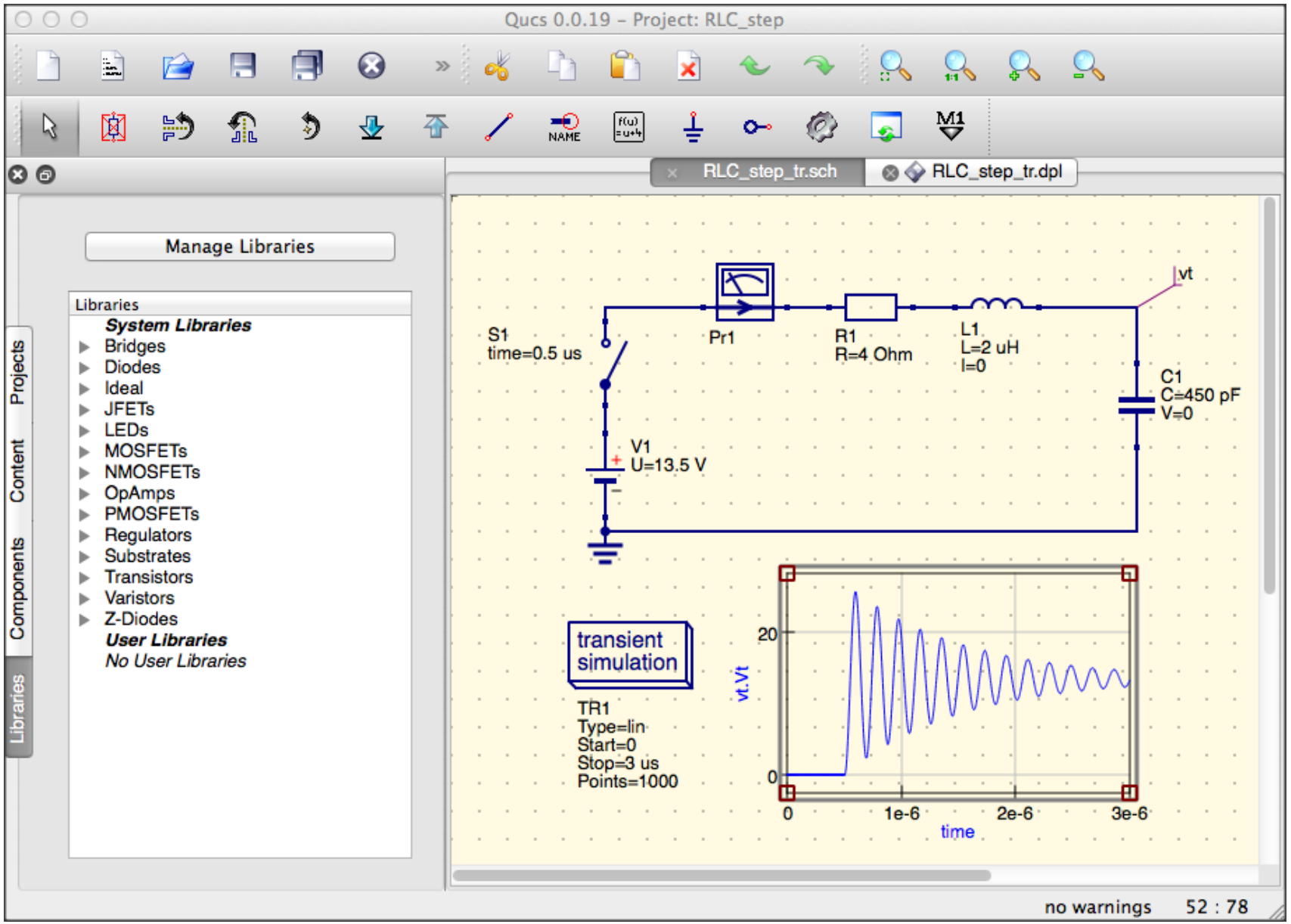
Contents


Qucs 0.0.19 – Project: RLC_step
RLC_step_tr.sch
RLC_step_tr.dpl
Content of RLC_step
Note
Others
Datasets
RLC_step_tr.dat
Data Displays
RLC_step_tr.dpl
Octave
Verilog
Verilog-A
VHDL
Schematics
RLC_step_tr.sch
Projects
Content
Components
Libraries
S1
time=0.5 us
Pr1
R1
R=4 Ohm
L1
L=2 uH
I=0
vt
C1
C=450 pF
V=0
V1
U=13.5 V
transient
simulation
TR1
Type=lin
Start=0
Stop=3 us
Points=1000
vt.Vt
20
0
0
1e-6
2e-6
3e-6
time
no warnings
65 : 35

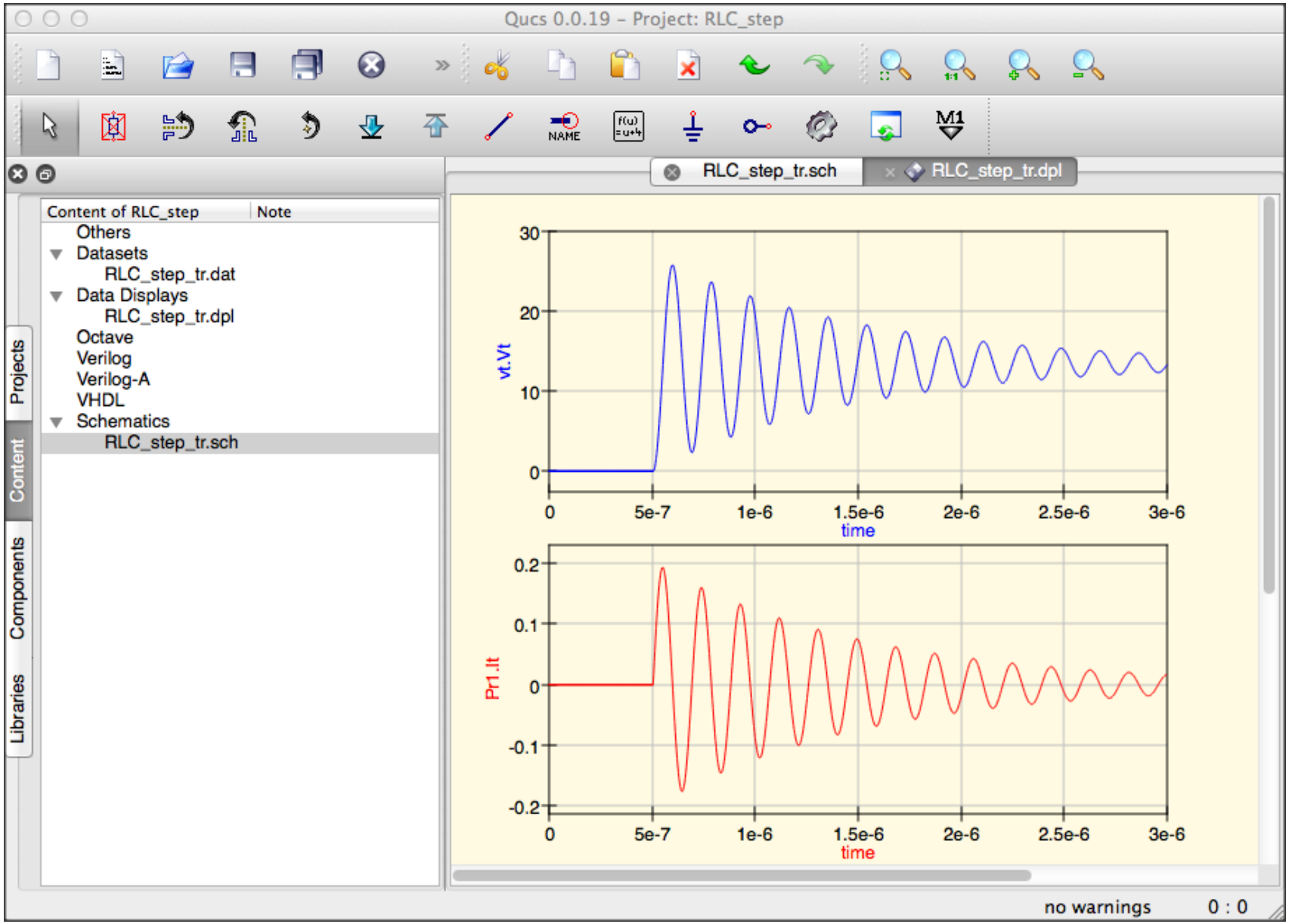
Components


Qucs 0.0.19 – Project: RLC_step
RLC_step_tr.sch
RLC_step_tr.dpl
lumped components
Resistor
Resistor US
Capacitor
Inductor
Ground
Subcircuit Port
Transformer
symmetric Tran...
Search Components
Clear
Projects
Content
Components
Libraries
S1
time=0.5 us
Pr1
R1
R=4 Ohm
L1
L=2 uH
I=0
vt
C1
C=450 pF
V=0
V1
U=13.5 V
transient
simulation
TR1
Type=lin
Start=0
Stop=3 us
Points=1000
vt.Vt
20
0
0
1e-6
2e-6
3e-6
time
no warnings
66 : 145

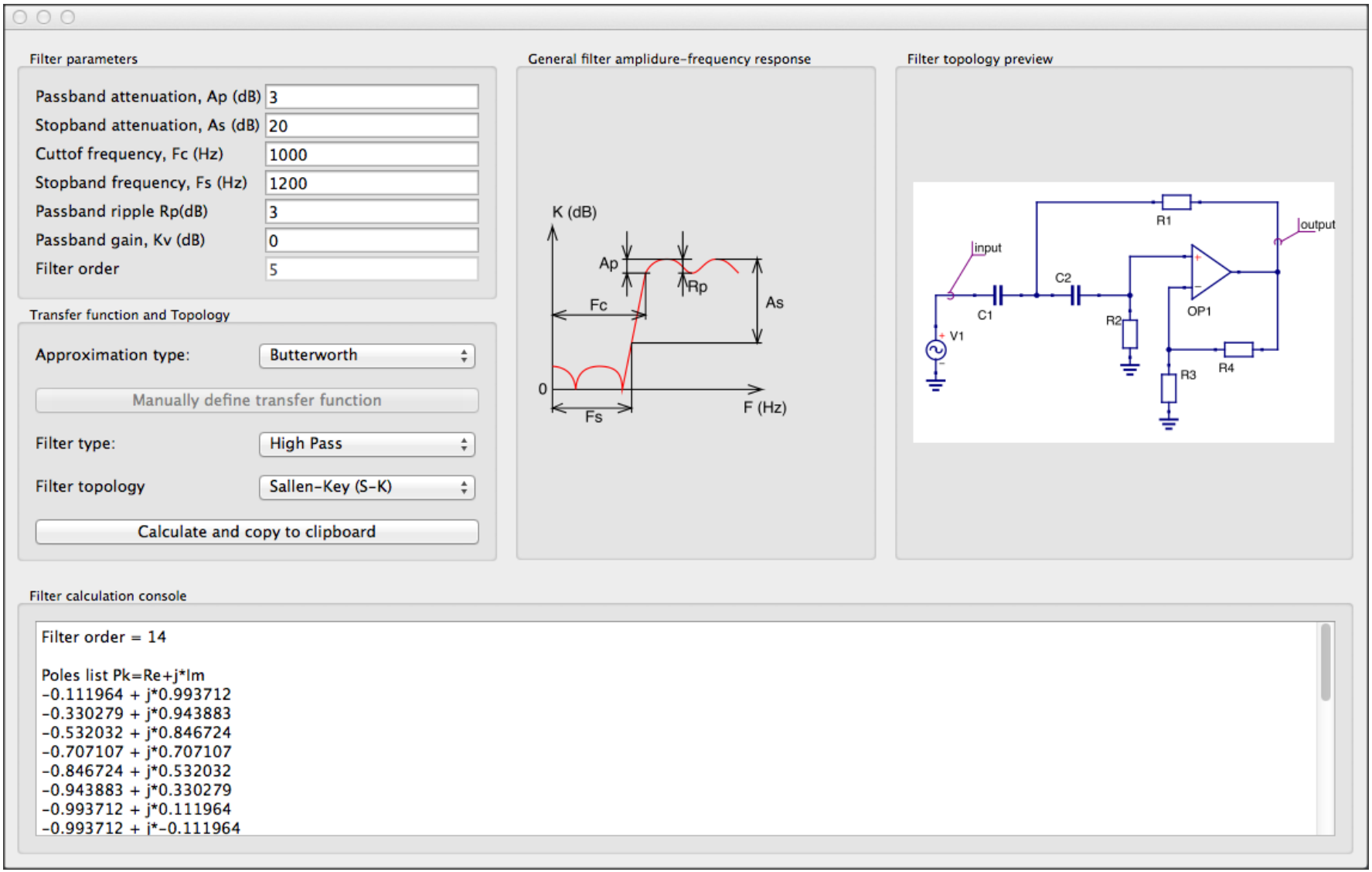
Libraries


Qucs 0.0.19 – Project: RLC_step
RLC_step_tr.sch
RLC_step_tr.dpl
Manage Libraries
Libraries
System Libraries
Bridges
Diodes
Ideal
JFETs
LEDs
MOSFETs
NMOSFETs
OpAmps
PMOSFETs
Regulators
Substrates
Transistors
Varistors
Z-Diodes
User Libraries
No User Libraries
Projects
Content
Components
Libraries
S1
time=0.5 us
Pr1
R1
R=4 Ohm
L1
L=2 uH
I=0
vt
C1
C=450 pF
V=0
V1
U=13.5 V
transient
simulation
TR1
Type=lin
Start=0
Stop=3 us
Points=1000
vt.Vt
20
0
0
1e-6
2e-6
3e-6
time
no warnings
52 : 78

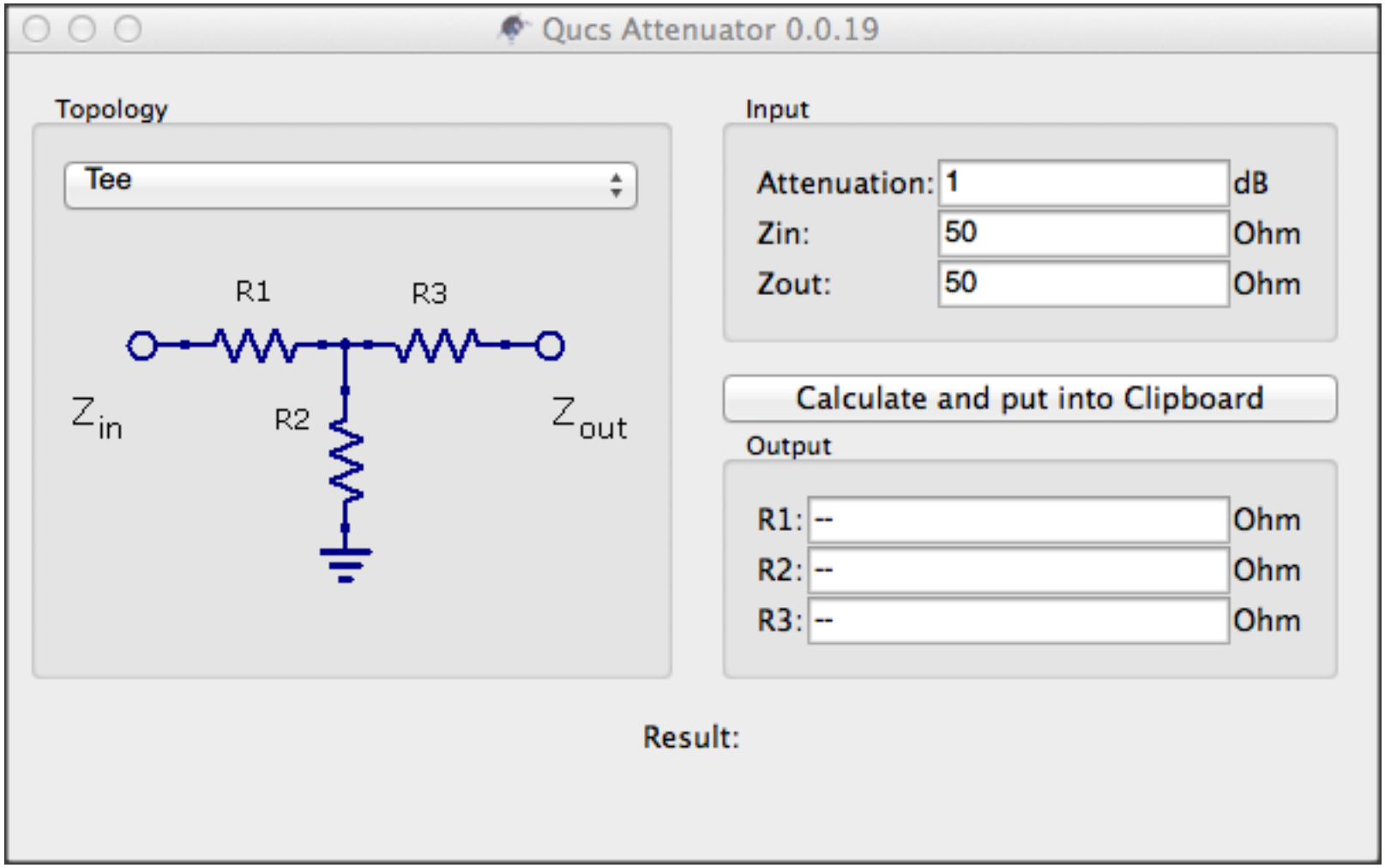
Visualization



Qucs-ActiveFilter



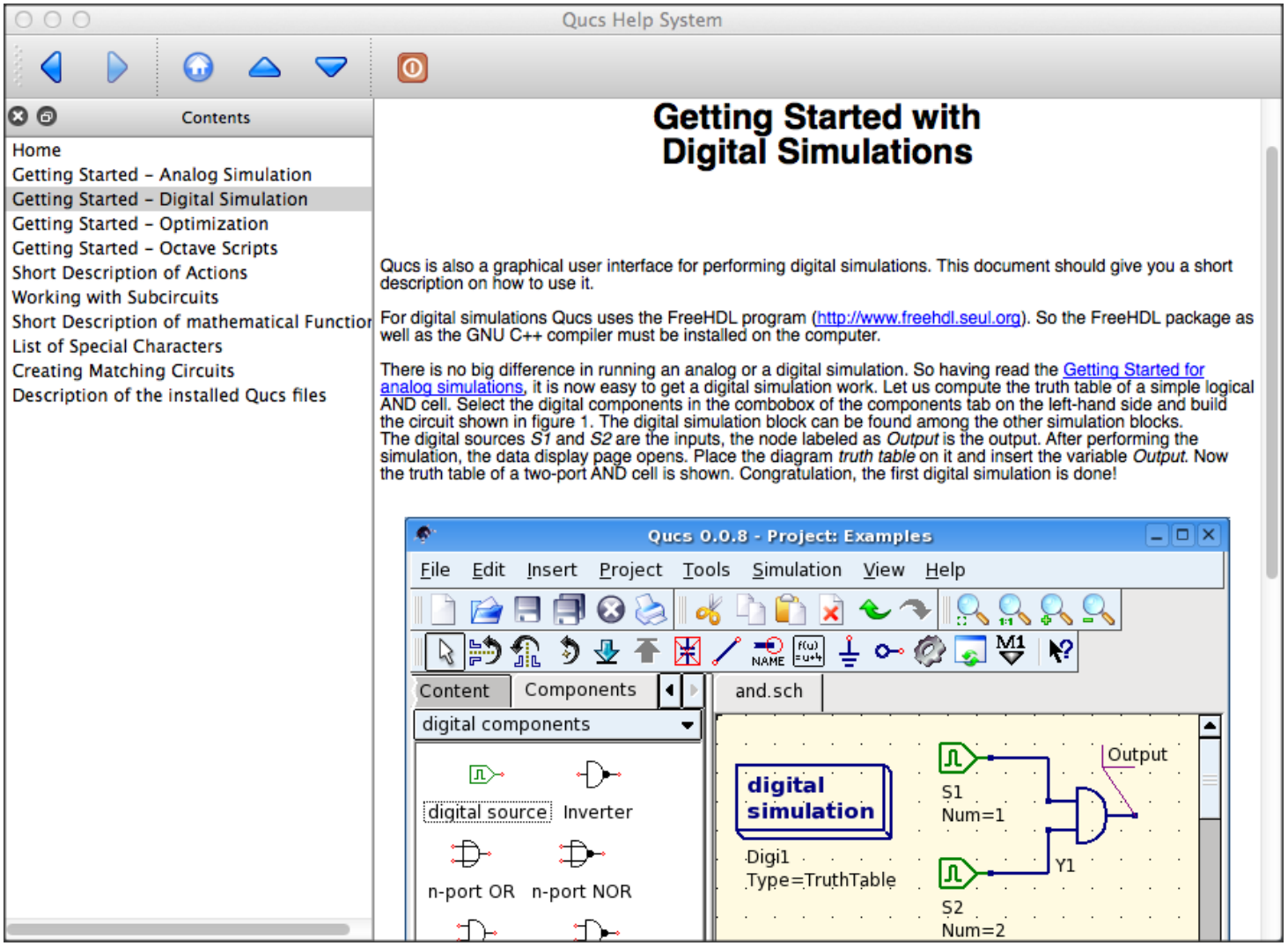
Qucs-Attenuator



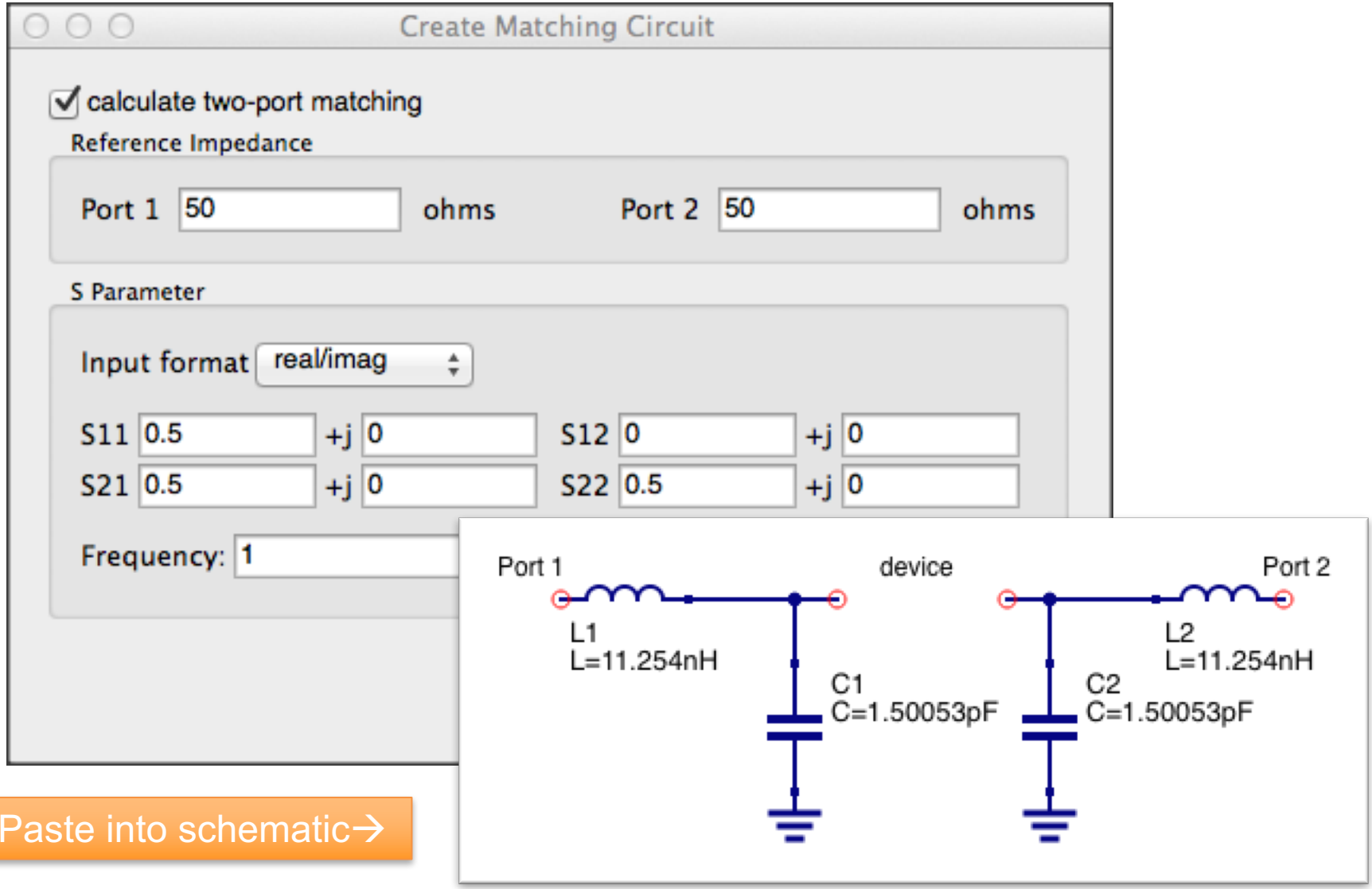
Qucs-Help

http://qucs-help.readthedocs.io/

DEPRECATED

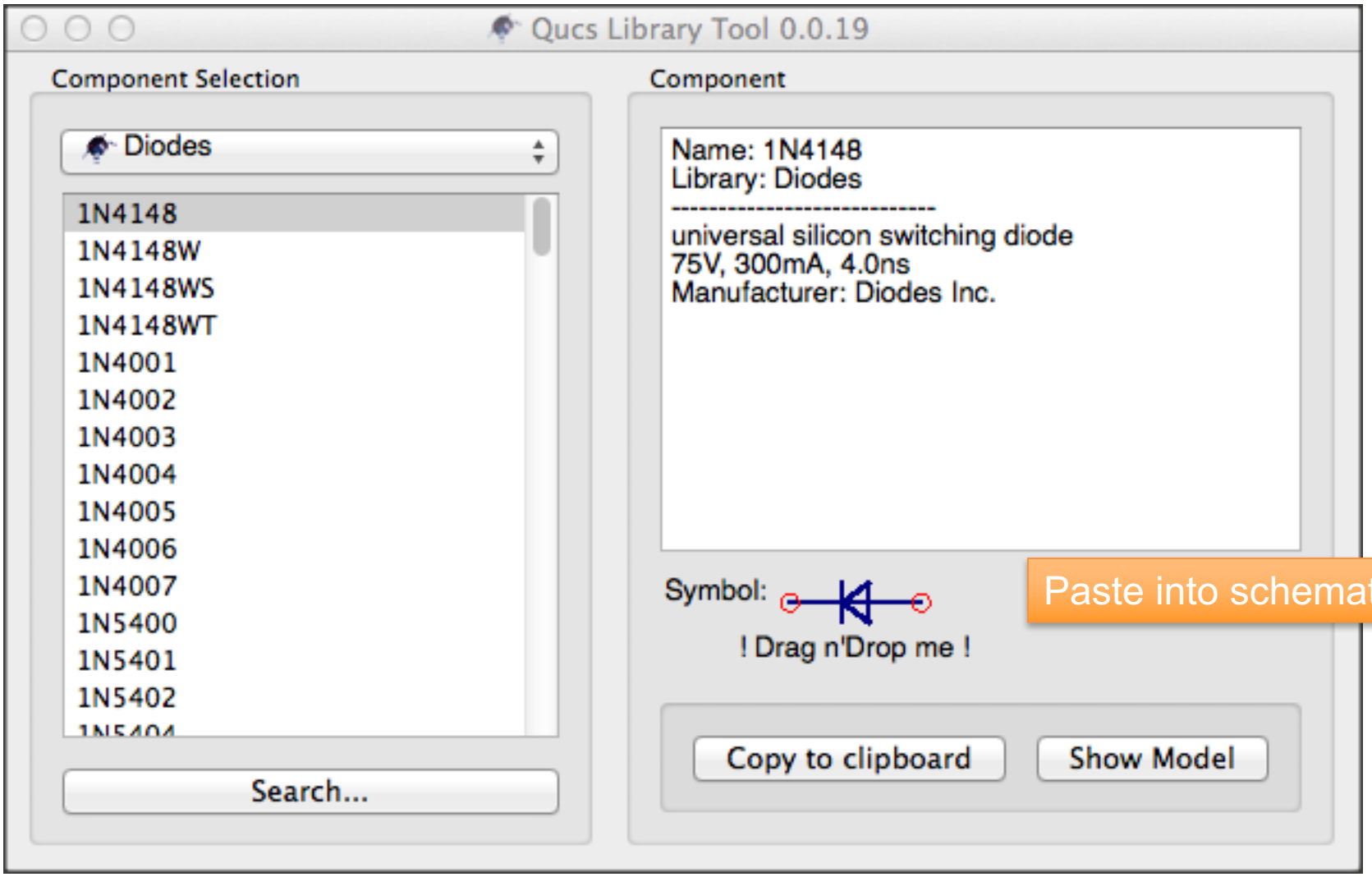


Qucs-Matching

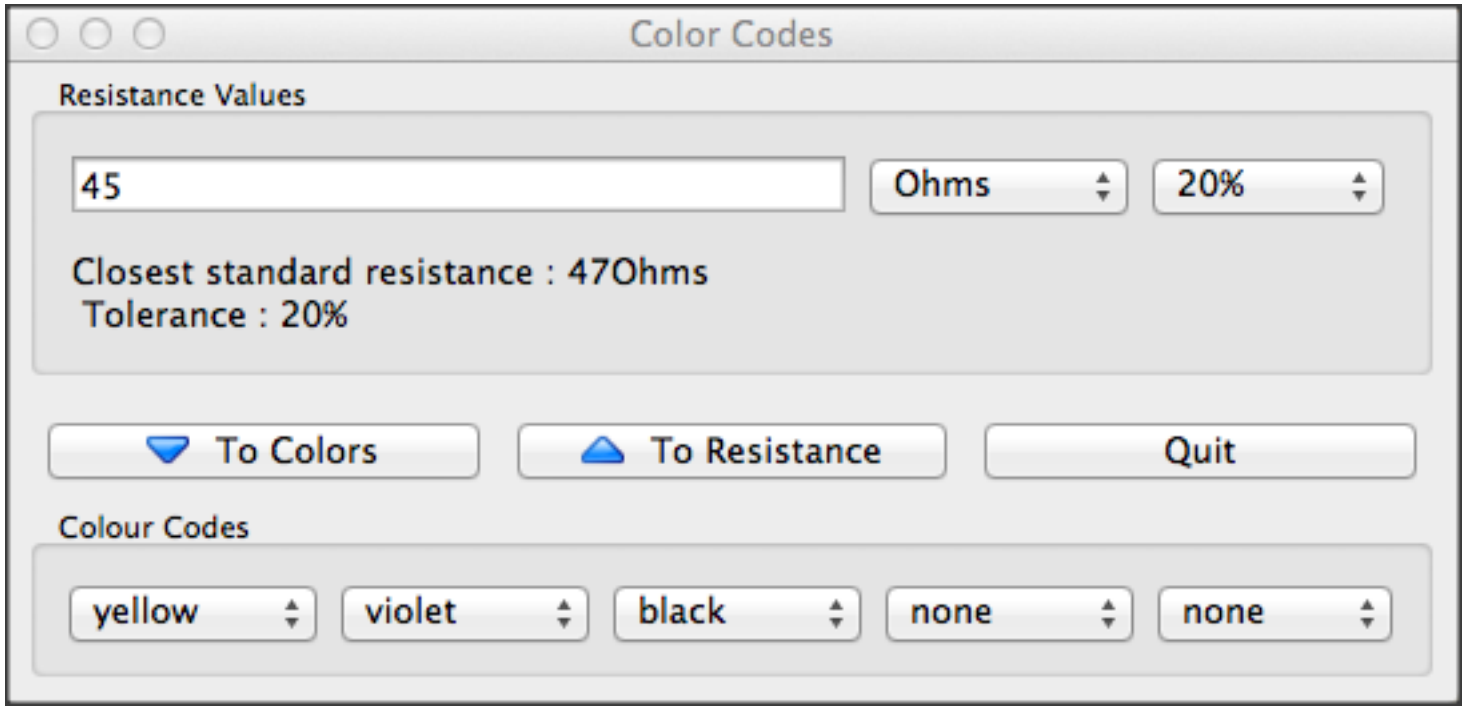


Paste into schematic→

Qucs-Lib

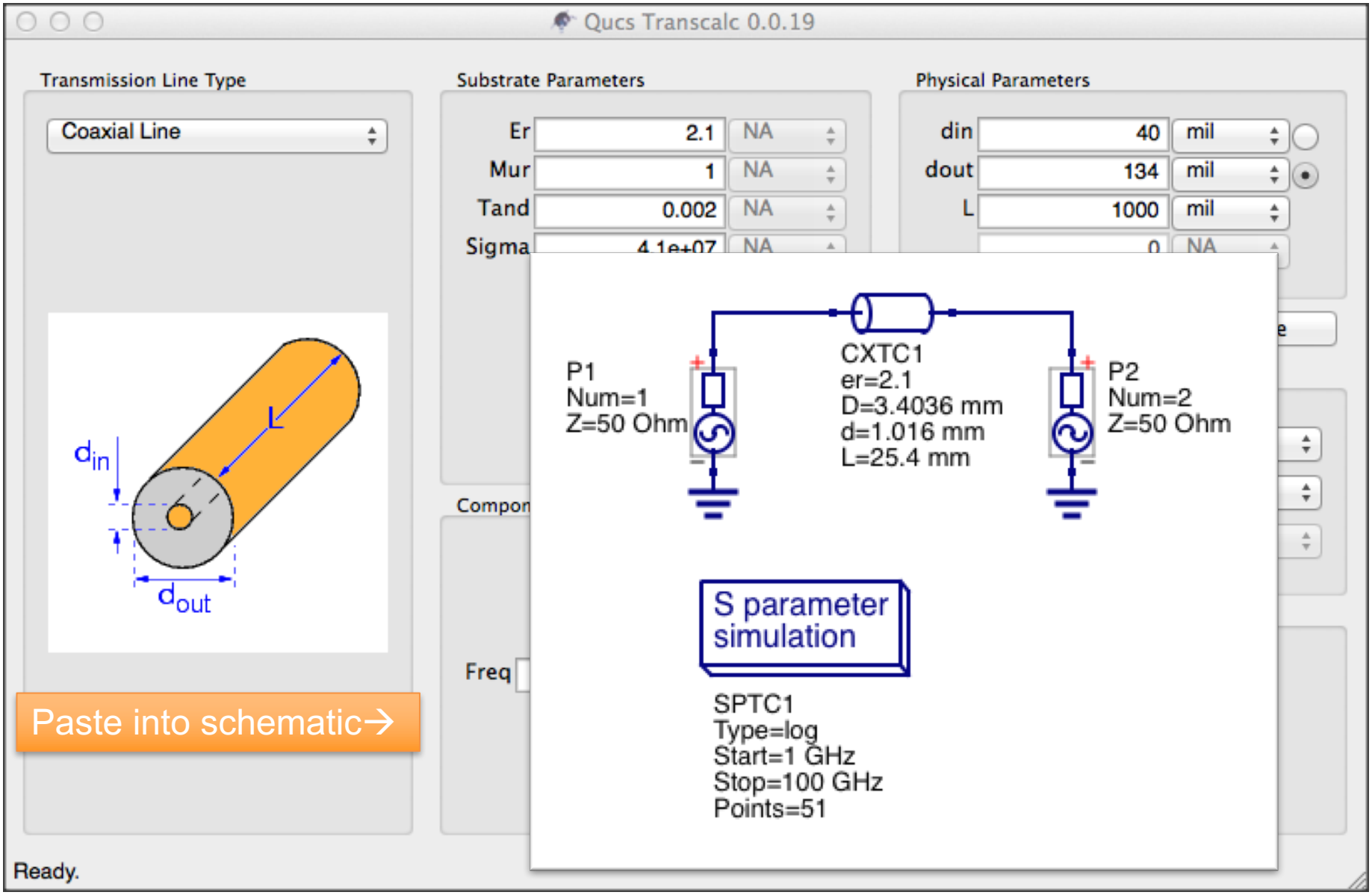

Qucs Library Tool 0.0.19
Component Selection
Diodes
1N4148
1N4148W
1N4148WS
1N4148WT
1N4001
1N4002
1N4003
1N4004
1N4005
1N4006
1N4007
1N5400
1N5401
1N5402
Search...
Component
Name: 1N4148
Library: Diodes
universal silicon switching diode
75V, 300mA, 4.0ns
Manufacturer: Diodes Inc.
Symbol:
! Drag n'Drop me !
Paste into schematic→
Copy to clipboard
Show Model

Qucs-Rescodes

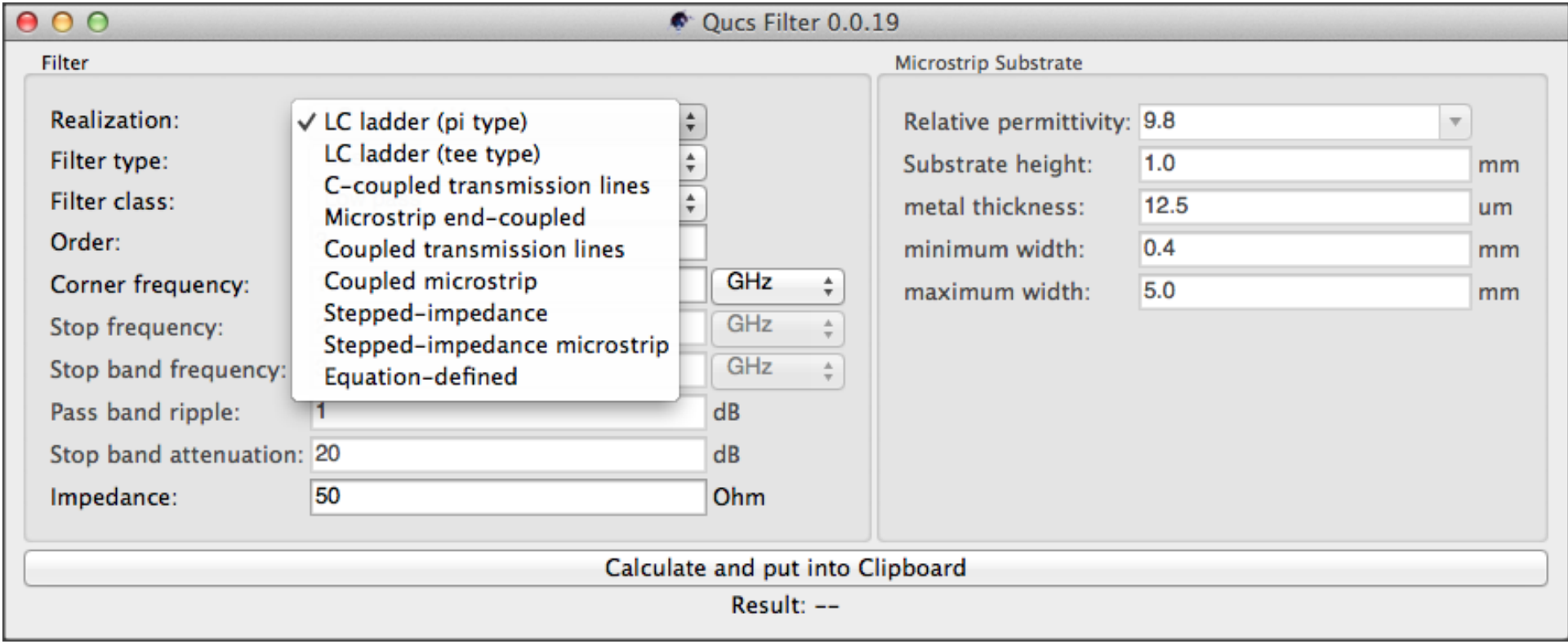


Paste into schematic→

Qucs-Transcalc



Qucs-Filter



Paste into schematic→

Command Line Tools

- Qucs – schematic
  - schematic to netlist
  - schematic to print
  - dump components data
- Qucsator – simulator
  - DC
  - Transient
  - AC
  - AC Noise
  - **S-Parameter**
  - S-Parameter Noise
  - (Harmonic Balance)

- Qucsconv - converter

```
spice       - qucs
spice       - qucslib
vcd         - qucsdata
qucsdata    - csv
qucsdata    - touchstone
citi        - qucsdata
touchstone  - qucsdata
csv         - qucsdata
zvr         - qucsdata
mdl         - qucsdata
qucsdata    - matlab
```

- Custom file formats
  - schematic
  - library
  - netlist
  - data file

Verilog-A

- Includes ~~53~~ 38 models written in Verilog-A (GPL)
- Compact models
  - ~~BSIM 3, 4, 6 (Berkeley)~~
  - EKV (EPFL)
  - ~~HICUM L0, L2 (TU-Dresden)~~
  - ~~FBH-HBT (TU-Berlin)~~

CMC license issues → qucs-nonfree repository

- ADMS (Automatic Device Model Synthesizer)
  - Verilog-A → XML transformations → "XYZ code"
  - Subset of Verilog-AMS

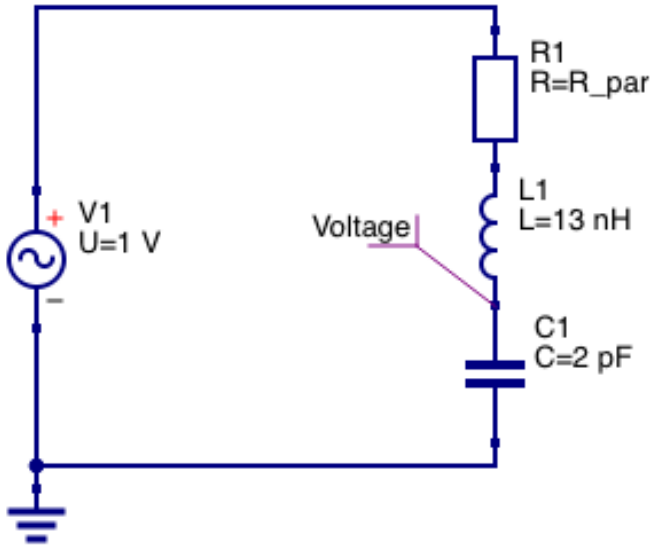
Accellera license issue → New .vams headers GPL3+

- QUCS limitations
  - Not supported: `V(n)<+ … ;`

Demo

- Examples
  - RLC circuit, parameter sweep
  - 555 timer: macro modeling
  - Optimization: Band-pass filter
  - 10 GHz microstrip band-pass filter
  - Verilog counter
  - Verilog-A support / model builder

RLC, parameter sweep



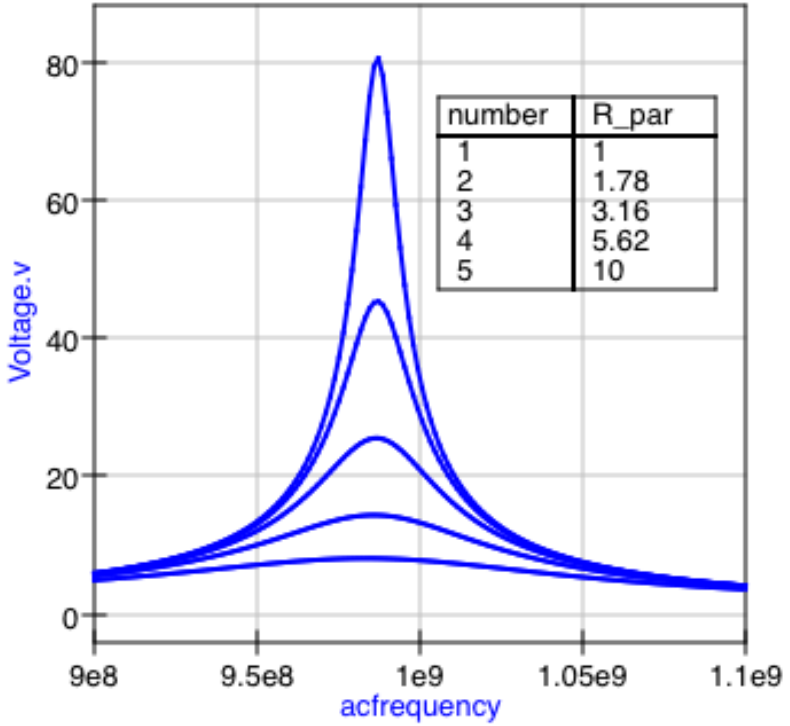
The voltage overshot strongly depends on the quality of the resonance circuit.

ac simulation

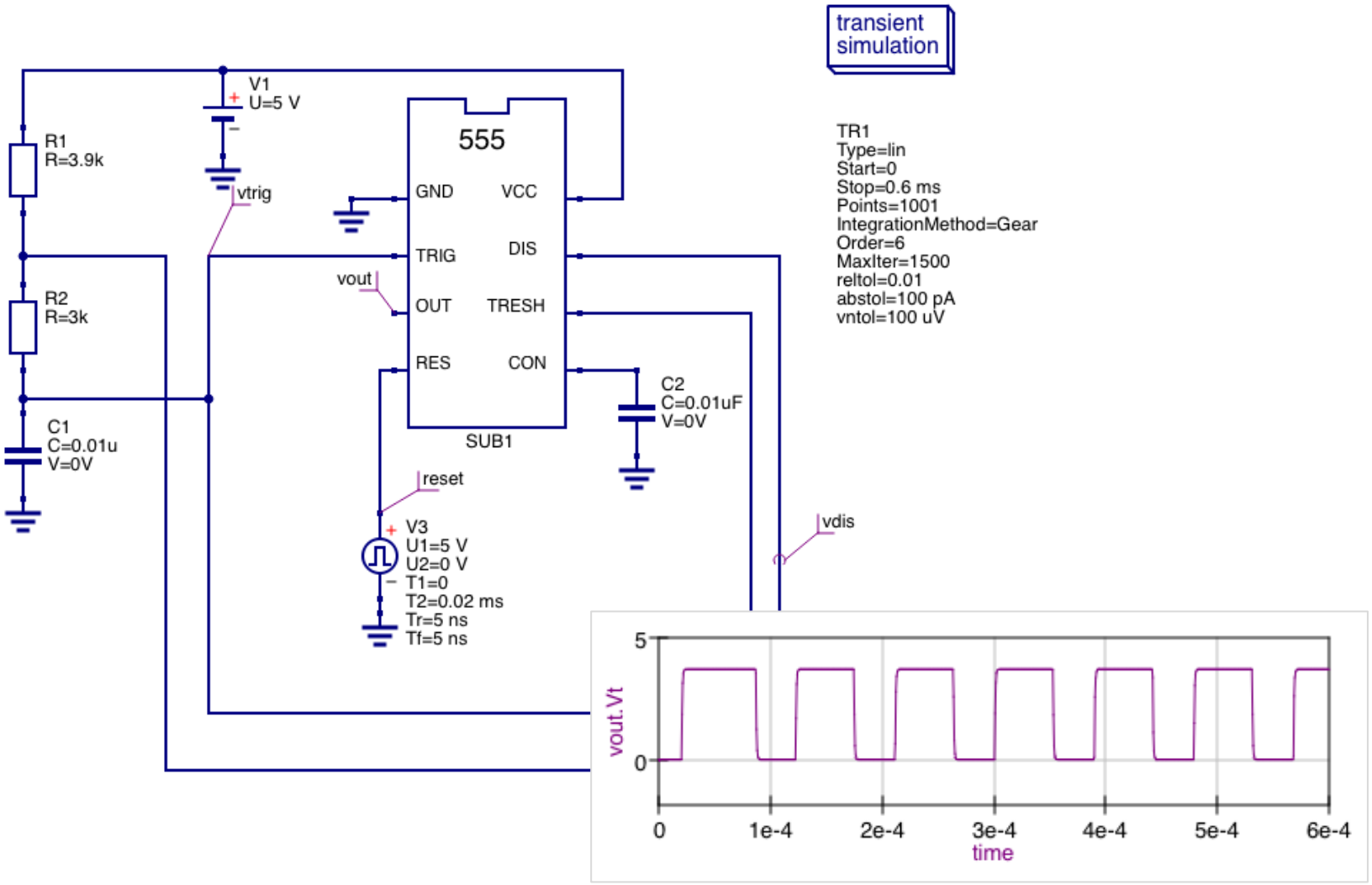
AC1
Type=lin
Start=0.9 GHz
Stop=1.1 GHz
Points=150

Parameter sweep

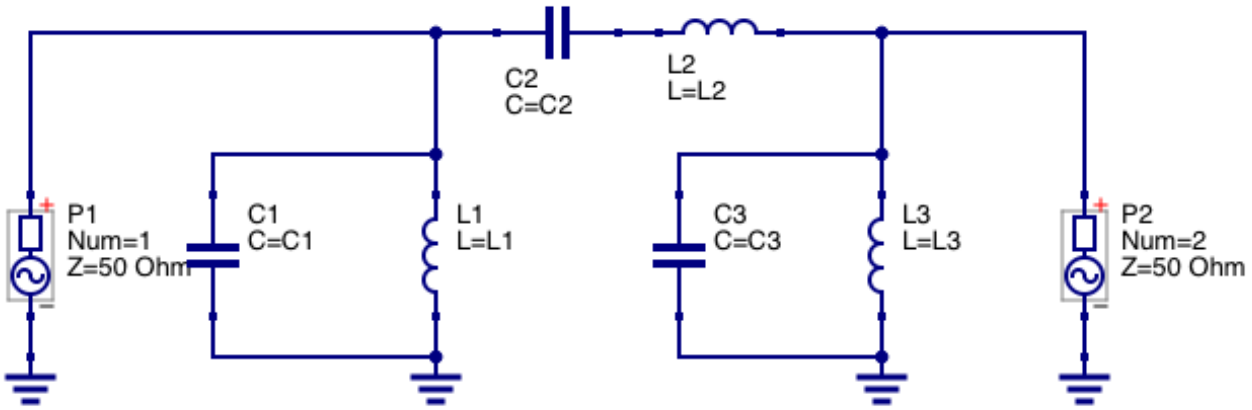
SW1
Sim=AC1
Type=log
Param=R_par
Start=1 Ohm
Stop=10 Ohm
Points=5



555 macro model

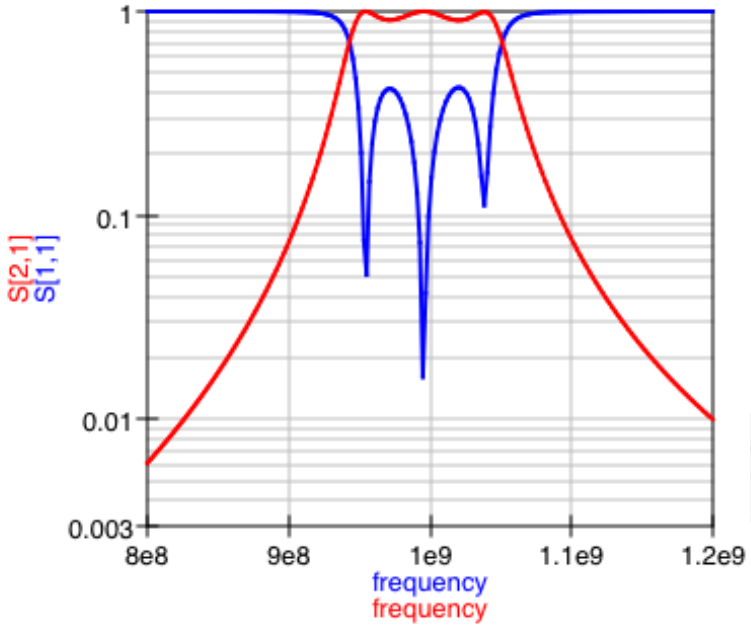


Optimization (ASCO)



S parameter simulation

SP1
Type=log
Start=800 MHz
Stop=1200 MHz
Points=200



Optimization

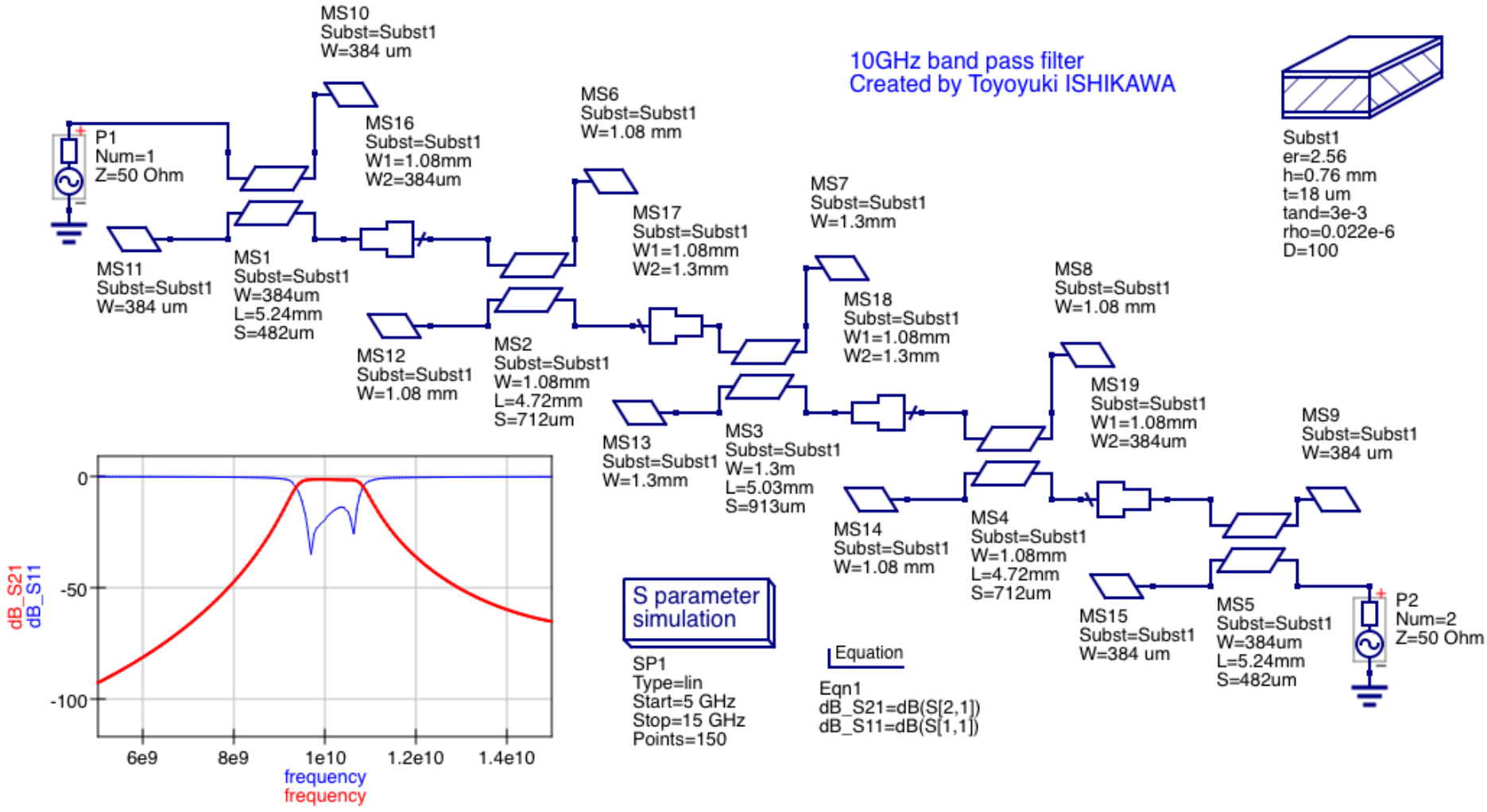
Opt1

Equation

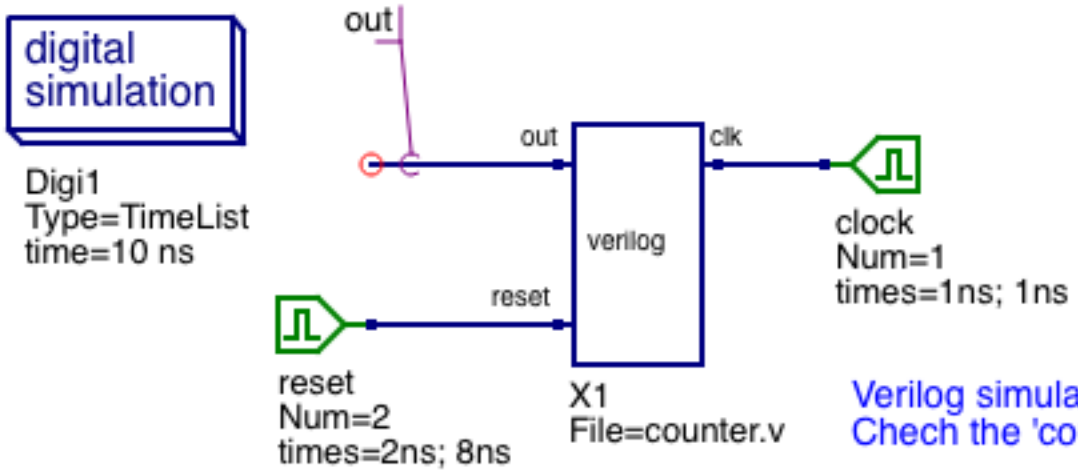
Eqn1
Left_Side_Lobe=max(dB(S[2,1]),800e6:900e6)
Pass_Band_Ripple=min(dB(S[2,1]),960e6:1040e6)
Right_Side_Lobe=max(dB(S[2,1]),1100e6:1200e6)
S11_In_Band=-max(dB(S[1,1]),960e6:1040e6)

number	Left_Side_Lobe	Pass_Band_Ripple	Right_Side_Lobe	S11_In_Band
1	-23.1	-0.856	-22.7	7.47

Microstrip band-pass filter

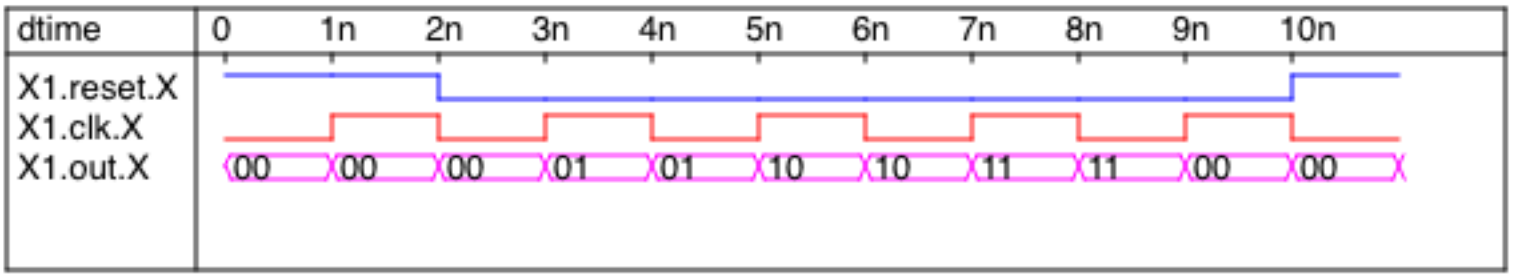


Verilog Counter




```
module counter(out, clk, reset);

  parameter WIDTH = 2;

  output [WIDTH-1 : 0] out;
  input                clk, reset;

  reg [WIDTH-1 : 0]    out;
  wire         clk, reset;

  always @(posedge clk)
    out <= out + 1;

  always @reset
    if (reset)
      assign out = 0;
    else
      deassign out;

endmodule // counter
```

Verilog simulation with Icarus Verilog
Chech the 'counter.v' for the HDL model.



Status

- Release 0.0.19 (January 22, 2017)
  - Bug fixing, usability improvements, build system cleanup
  - Ongoing port Qt3Support to Qt4
  - New active-filter synthesis tool
  - Integration of regression tests
  - Removal of non-GPL models
  - Adopted git-flow branching model
  - 168 issues closed
- Develop (Release 0.0.20)
  - RF and Microwave
  - Tuner
  - Removal of qucs-editor and qucs-help
  - … (quick release)

Resources

- Website: http://qucs.sourceforge.net/
- GitHub (preferred): https://github.com/Qucs/qucs/
- SourceForge: http://sourceforge.net/p/qucs/git/
- Mailing lists: http://sourceforge.net/p/qucs/mailman/
- IRC channel: #qucs
- Forum: http://sourceforge.net/p/qucs/discussion/
- Bug trackers:
  - https://github.com/Qucs/qucs/issues
  - http://sourceforge.net/p/qucs/_list/tickets
- Source code documentation:
  - http://qucs.github.io/qucs-doxygen/qucs/index.html
  - http://qucs.github.io/qucs-doxygen/qucs-core/index.html
- Downloads: http://sourceforge.net/projects/qucs/files/
- (NEW) Qucs-Help: http://qucs-help.readthedocs.io/
- (NEW) Transifex translations:
  - https://www.transifex.com/projects/p/qucs-desktop/
  - https://www.transifex.com/projects/p/qucs-help/

Final remarks

- User friendly
- Advanced components and modeling features
- We are open for collaboration
- Help is welcome