



QUCS

Quite Universal Circuit Simulator

Overview and Status

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FOSDEM 2017

EDA Developer room

Brussels, 04 February 2016



Qucs /kju:ks/

- Overview
 - Project background
 - Features
- Status
 - Development
 - Next release
- Final Remarks

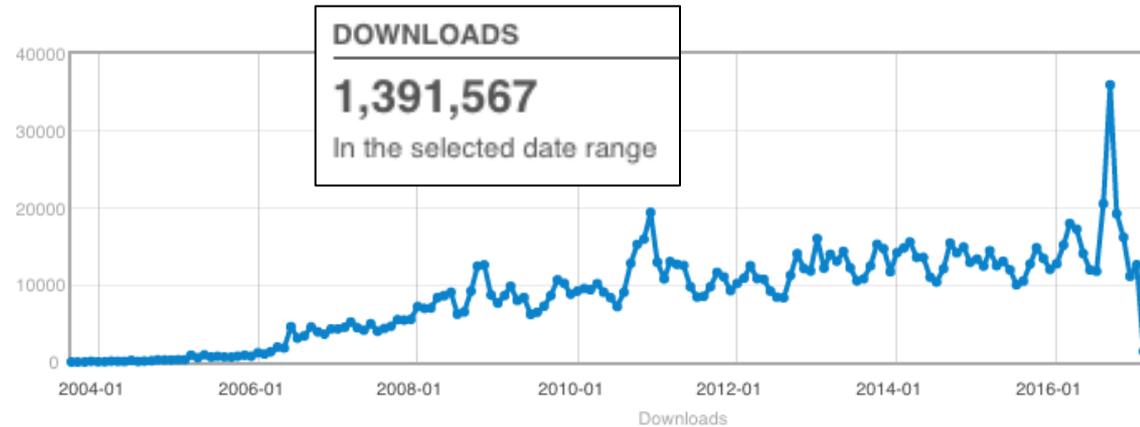
Project background



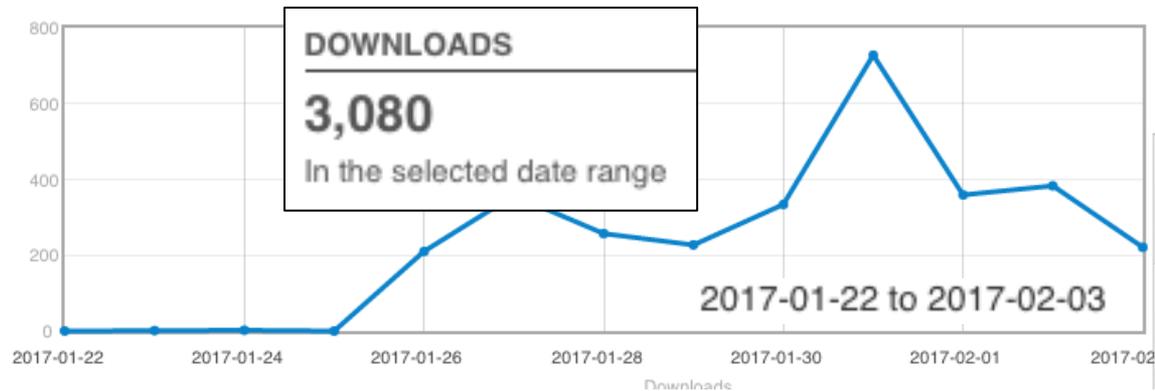
Website counter
1460126
visitors since 2005/04/27

- Created at TU-Berlin
 - Michael Margraf
 - Stefan Jahn
- GPLv2+
- 20+ contributors
- 20 languages
- Cross-platform
- Users
 - Education
 - Research
 - Hobbyists
 - Industry

- 2003 to 2017



- Qucs 0.0.19 - Windows





Main Features

- Schematic capture
- Simulator
- Data visualization
- Equation system
- Component library
- Design / synthesis tools
- Modeling tools
 - Spice converter (limited)
 - Equation defined device (EDD)
 - Verilog-A model builder
- Post-processing
 - Octave/MATLAB
 - Python
- Dependencies
 - C++ compiler
 - Qt4 (with Qt3Support)
 - Autotools / CMake
 - gperf / flex / bison
 - ADMS
 - LaTeX

Experimental



- Qucs-S
 - SPICE support
 - Ngspice, Xyce, SpiceOpus
 - Verilog-A generators
 - XSPICE generators
 - ...
- Gnucsator
 - gnuicap based qucsator implementation
- QUCS → gschem

<https://ra3xdh.github.io/>

<https://github.com/Qucs/gnucsator>

<https://github.com/erichVK5/translate2geda/>



Support

- Website
 - <http://qucs.sourceforge.net>
- Active maintainers:
 - Guilherme Brondani Torri
 - Claudio Girardi
 - Vadim Kuznetsov
 - Felix Salfelder
 - Andrés Martínez Mera
 - Mike Brinson
- Documentation
 - Help
 - Tutorial Workbook
 - Report Workbook
 - Technical Manual
- SourceForge
 - Binaries
 - Git repository (mirror)
 - Issue tracker
 - Forum / mailing lists
- GitHub
 - Git repository (preferred)
 - Issue tracker
 - Wiki
 - Travis CI
 - AppVeyor



Tools

- Graphical Interface
 - Qucs
 - ActiveFilter
 - Attenuator
 - Editor
 - Filter
 - Help
 - Matching
 - Library
 - Rescodes
 - Transcalc
- ~ 170 components
- Command Line
 - qucs
 - qucsator
 - qucsconv
- Third-party and scripts
 - asco
 - admsXml
 - iverilog
 - freehdl
 - ps2sp
 - octave
 - python



Projects

Qucs 0.0.19 - Project: RLC_step

RLC_step_tr.sch RLC_step_tr.dpl

New Open Delete

- _devel_bsim6_inverter_transient_p
- _devel_ngspice_prj
- 555_examples_prj
- AC_SW_resonance_prj
- asco_optimize_prj
- chaos_prj
- DC_AC_active_lp_prj
- octave_example_prj
- RLC_step_prj**
- series_rlc_prj
- SP_BFP405_prj
- SP_bpf_10Ghz_prj
- testset_prj
- testset_small_prj
- total_resistor_prj
- TR_boostconverter_prj
- TR_colpitts_base_prj
- TR_diode_hb_prj
- TR_gilbert_prj
- TR_multiplier_prj
- va_loader_test_prj
- verilog_counter_prj

S1
time=0.5 us

Pr1

R1
R=4 Ohm

L1
L=2 uH
I=0

V1
U=13.5 V

C1
C=450 pF
V=0

vt

transient simulation

TR1
Type=lin
Start=0
Stop=3 us
Points=1000

vt

time

no warnings 49 : 51

Contents



Qucs 0.0.19 - Project: RLC_step

Content of RLC_step

- Others
- ▼ Datasets
 - RLC_step_tr.dat
- ▼ Data Displays
 - RLC_step_tr.dpl
- Octave
- Verilog
- Verilog-A
- VHDL
- ▼ Schematics
 - RLC_step_tr.sch

RLC_step_tr.sch

S1 time=0.5 us

V1 U=13.5 V

Pr1

R1 R=4 Ohm

L1 L=2 uH I=0

C1 C=450 pF V=0

vt

transient simulation

TR1
Type=lin
Start=0
Stop=3 us
Points=1000

vt.Vt

time

no warnings 65 : 35

Components



Qucs 0.0.19 - Project: RLC_step

RLC_step_tr.sch RLC_step_tr.dpl

lumped components

- Resistor
- Resistor US
- Capacitor
- Inductor
- Ground
- Subcircuit Port
- Transformer
- symmetric Tran...

Search Components Clear

S1 time=0.5 us

Pr1

R1 R=4 Ohm

L1 L=2 uH I=0

V1 U=13.5 V

C1 C=450 pF V=0

vt

transient simulation

TR1
Type=lin
Start=0
Stop=3 us
Points=1000

vt.Vt

time

no warnings 66 : 145



Libraries

Qucs 0.0.19 - Project: RLC_step

Manage Libraries

Libraries

- System Libraries**
 - ▶ Bridges
 - ▶ Diodes
 - ▶ Ideal
 - ▶ JFETs
 - ▶ LEDs
 - ▶ MOSFETs
 - ▶ NMOSFETs
 - ▶ OpAmps
 - ▶ PMOSFETs
 - ▶ Regulators
 - ▶ Substrates
 - ▶ Transistors
 - ▶ Varistors
 - ▶ Z-Diodes
- User Libraries**
 - No User Libraries

RLC_step_tr.sch RLC_step_tr.dpl

S1 time=0.5 us

Pr1

R1 R=4 Ohm

L1 L=2 uH I=0

V1 U=13.5 V

C1 C=450 pF V=0

vt

transient simulation

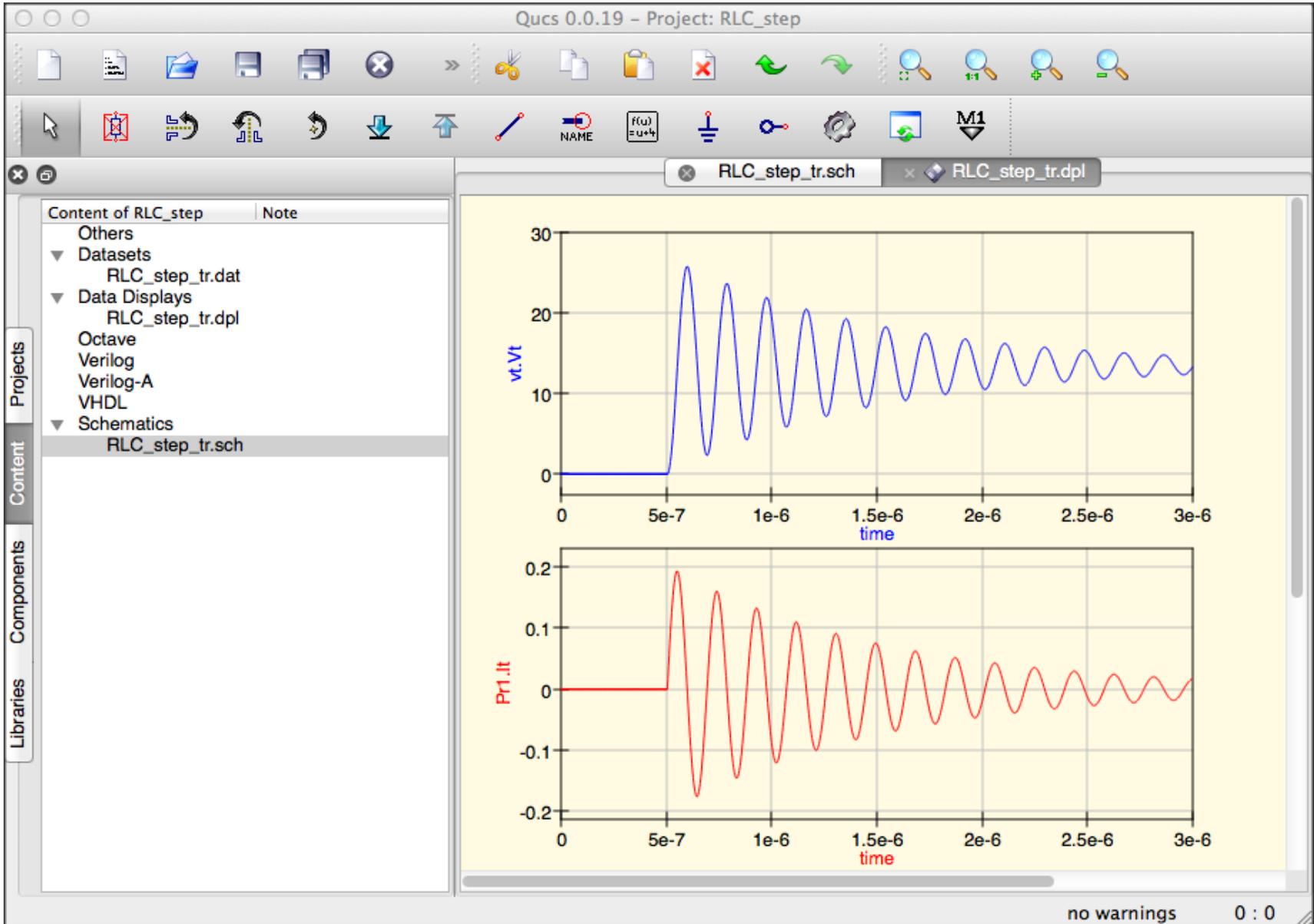
TR1
Type=lin
Start=0
Stop=3 us
Points=1000

vt.Vt

time

no warnings 52 : 78

Visualization



Qucs-ActiveFilter



Filter parameters

Passband attenuation, A_p (dB)	3
Stopband attenuation, A_s (dB)	20
Cutoff frequency, F_c (Hz)	1000
Stopband frequency, F_s (Hz)	1200
Passband ripple R_p (dB)	3
Passband gain, K_v (dB)	0
Filter order	5

Transfer function and Topology

Approximation type:

Filter type:

Filter topology:

General filter amplitude-frequency response

The graph plots gain K (dB) on the vertical axis against frequency F (Hz) on the horizontal axis. Key parameters are marked: A_p (passband attenuation), R_p (passband ripple), A_s (stopband attenuation), F_c (cutoff frequency), and F_s (stopband frequency). The curve shows a high-pass filter response with a passband ripple of 3 dB and a stopband attenuation of 20 dB.

Filter topology preview

The circuit diagram shows a Sallen-Key active filter topology. It consists of an input terminal connected to a voltage source V_1 through capacitor C_1 . The signal then passes through capacitor C_2 to the non-inverting input of an operational amplifier OP_1 . The inverting input of OP_1 is connected to a voltage divider formed by resistors R_2 and R_3 . The feedback path from the output to the inverting input consists of resistors R_1 and R_4 . The output is labeled "output".

Filter calculation console

Filter order = 14

Poles list $P_k = Re + j*Im$

- 0.111964 + j*0.993712
- 0.330279 + j*0.943883
- 0.532032 + j*0.846724
- 0.707107 + j*0.707107
- 0.846724 + j*0.532032
- 0.943883 + j*0.330279
- 0.993712 + j*0.111964
- 0.993712 + j*-0.111964

Qucs-Attenuator



Qucs Attenuator 0.0.19

Topology

Tee

Input

Attenuation: 1 dB

Zin: 50 Ohm

Zout: 50 Ohm

Calculate and put into Clipboard

Output

R1: -- Ohm

R2: -- Ohm

R3: -- Ohm

Result:



Qucs-Help

<http://qucs-help.readthedocs.io/>

DEPRECATED



Getting Started with Digital Simulations

Qucs is also a graphical user interface for performing digital simulations. This document should give you a short description on how to use it.

For digital simulations Qucs uses the FreeHDL program (<http://www.freehdl.seul.org>). So the FreeHDL package as well as the GNU C++ compiler must be installed on the computer.

There is no big difference in running an analog or a digital simulation. So having read the [Getting Started for analog simulations](#), it is now easy to get a digital simulation work. Let us compute the truth table of a simple logical AND cell. Select the digital components in the combobox of the components tab on the left-hand side and build the circuit shown in figure 1. The digital simulation block can be found among the other simulation blocks. The digital sources *S1* and *S2* are the inputs, the node labeled as *Output* is the output. After performing the simulation, the data display page opens. Place the diagram *truth table* on it and insert the variable *Output*. Now the truth table of a two-port AND cell is shown. Congratulations, the first digital simulation is done!

Qucs 0.0.8 - Project: Examples

File Edit Insert Project Tools Simulation View Help

Content Components and.sch

digital components

digital source Inverter

n-port OR n-port NOR

digital simulation

.Digi1
.Type=TruthTable

S1 Num=1

S2 Num=2

Output

Y1

Qucs-Matching



Create Matching Circuit

calculate two-port matching

Reference Impedance

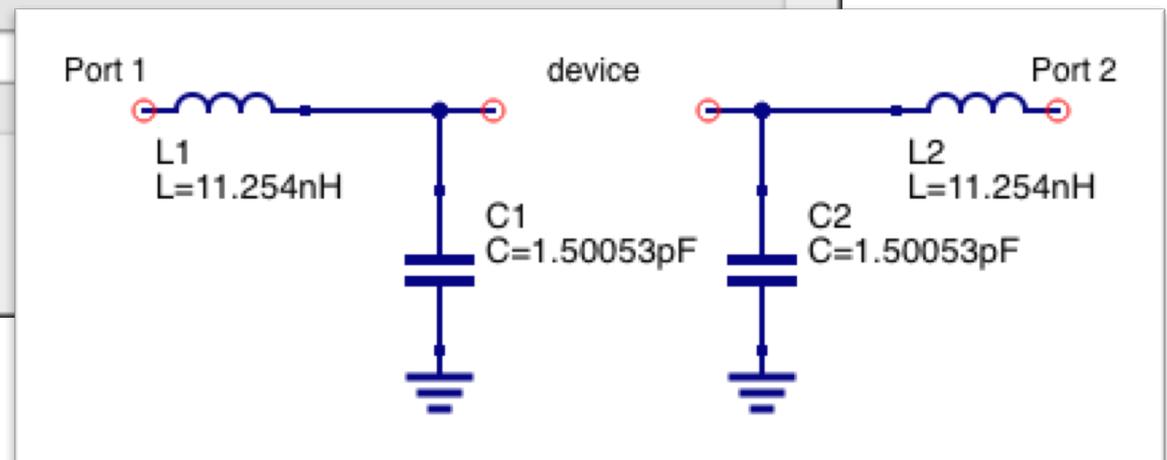
Port 1 ohms Port 2 ohms

S Parameter

Input format

S11	<input type="text" value="0.5"/>	+j	<input type="text" value="0"/>	S12	<input type="text" value="0"/>	+j	<input type="text" value="0"/>
S21	<input type="text" value="0.5"/>	+j	<input type="text" value="0"/>	S22	<input type="text" value="0.5"/>	+j	<input type="text" value="0"/>

Frequency:



Paste into schematic→

Qucs-Lib



Qucs Library Tool 0.0.19

Component Selection

Diodes

- 1N4148
- 1N4148W
- 1N4148WS
- 1N4148WT
- 1N4001
- 1N4002
- 1N4003
- 1N4004
- 1N4005
- 1N4006
- 1N4007
- 1N5400
- 1N5401
- 1N5402
- 1N5404

Search...

Component

Name: 1N4148
Library: Diodes

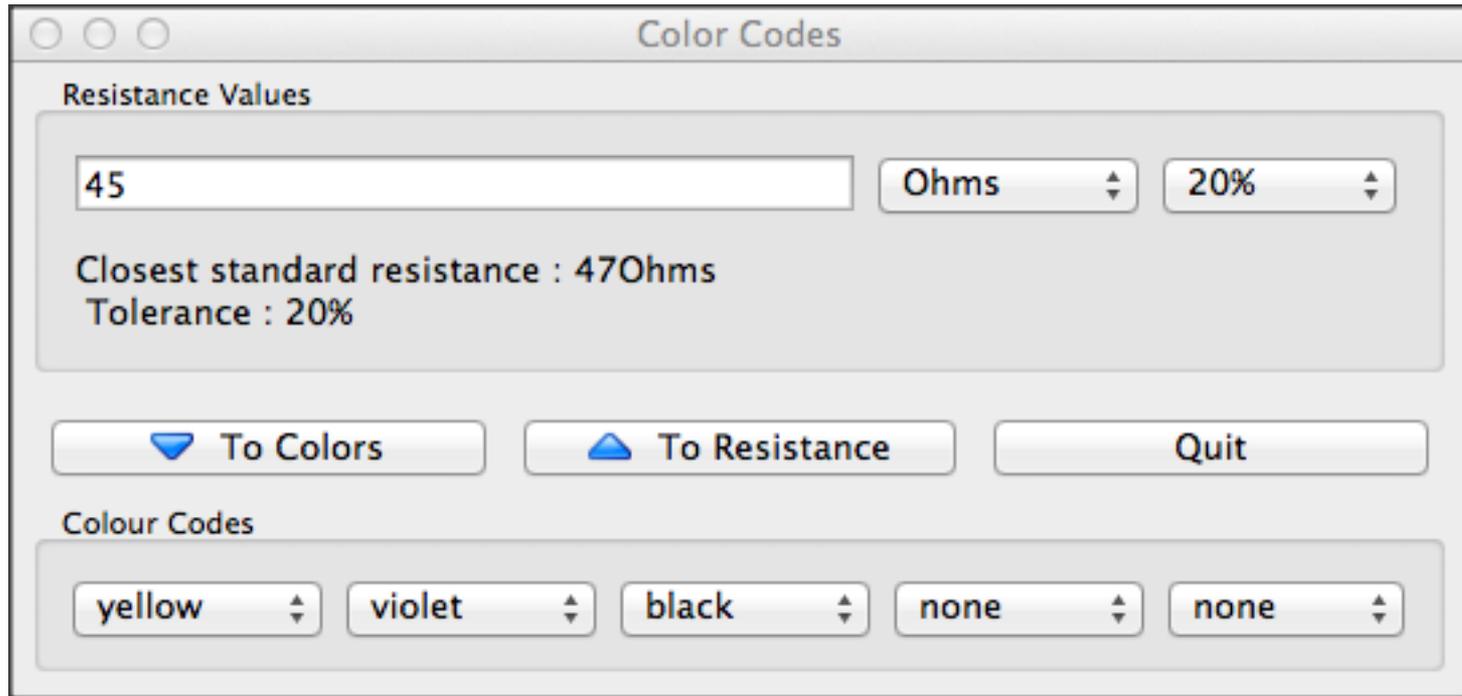
universal silicon switching diode
75V, 300mA, 4.0ns
Manufacturer: Diodes Inc.

Symbol:  ! Drag n'Drop me !

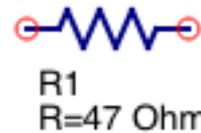
Paste into schematic →

Copy to clipboard Show Model

Qucs-Rescodes



Paste into schematic →



Qucs-Transcalc



Qucs Transcalc 0.0.19

Transmission Line Type: Coaxial Line

Substrate Parameters:

Er	2.1	NA
Mur	1	NA
Tand	0.002	NA
Sigma	4.1e+07	NA

Physical Parameters:

din	40	mil
dout	134	mil
L	1000	mil
	0	NA

Ready.

Paste into schematic →

S parameter simulation

Schematic diagram showing a transmission line component (CXTC1) connected between two ports (P1 and P2). P1 has Num=1 and Z=50 Ohm. P2 has Num=2 and Z=50 Ohm. The component parameters are: er=2.1, D=3.4036 mm, d=1.016 mm, L=25.4 mm. The simulation is an S parameter simulation with Type=log, Start=1 GHz, Stop=100 GHz, and Points=51.

Qucs-Filter



Qucs Filter 0.0.19

Filter

Realization: LC ladder (pi type) LC ladder (tee type) C-coupled transmission lines Microstrip end-coupled Coupled transmission lines Coupled microstrip Stepped-impedance Stepped-impedance microstrip Equation-defined

Filter type:

Filter class:

Order:

Corner frequency: GHz

Stop frequency: GHz

Stop band frequency: GHz

Pass band ripple: 1 dB

Stop band attenuation: 20 dB

Impedance: 50 Ohm

Microstrip Substrate

Relative permittivity: 9.8

Substrate height: 1.0 mm

metal thickness: 12.5 um

minimum width: 0.4 mm

maximum width: 5.0 mm

Calculate and put into Clipboard

Result: --

Paste into schematic →



Command Line Tools

- Qucs – schematic
 - schematic to netlist
 - schematic to print
 - dump components data
- Qucsator – simulator
 - DC
 - Transient
 - AC
 - AC Noise
 - **S-Parameter**
 - S-Parameter Noise
 - (Harmonic Balance)
- Qucsconv - converter
 - spice - qucs
 - spice - qucslib
 - vcd - qucsdata
 - qucsdata - csv
 - qucsdata - touchstone
 - citi - qucsdata
 - touchstone - qucsdata
 - csv - qucsdata
 - zvr - qucsdata
 - mdl - qucsdata
 - qucsdata - matlab
- Custom file formats
 - schematic
 - library
 - netlist
 - data file



Verilog-A

- Includes ~~53~~ 38 models written in Verilog-A (GPL)
- Compact models
 - ~~BSIM 3, 4, 6~~ (Berkeley) **CMC license issues**  qucs-nonfree repository
 - EKV (EPFL)
 - ~~HICUM L0, L2~~ (TU-Dresden)
 - ~~FBH-HBT~~ (TU-Berlin)
- ADMS (Automatic Device Model Synthesizer) **Accellera license issue**
 - Verilog-A → XML transformations → “XYZ code”
 - Subset of Verilog-AMS
- QUCS limitations
 - Not supported: $V(n) <+ \dots ;$

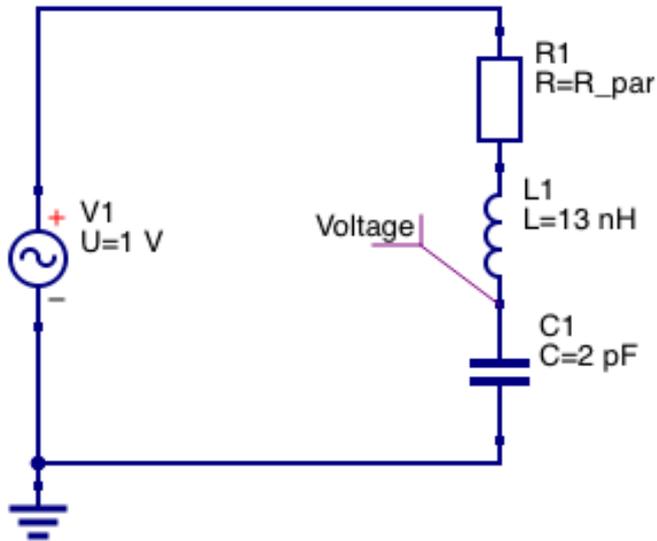
New .vams headers
GPL3+



Demo

- Examples
 - RLC circuit, parameter sweep
 - 555 timer: macro modeling
 - Optimization: Band-pass filter
 - 10 GHz microstrip band-pass filter
 - Verilog counter
 - Verilog-A support / model builder

RLC, parameter sweep



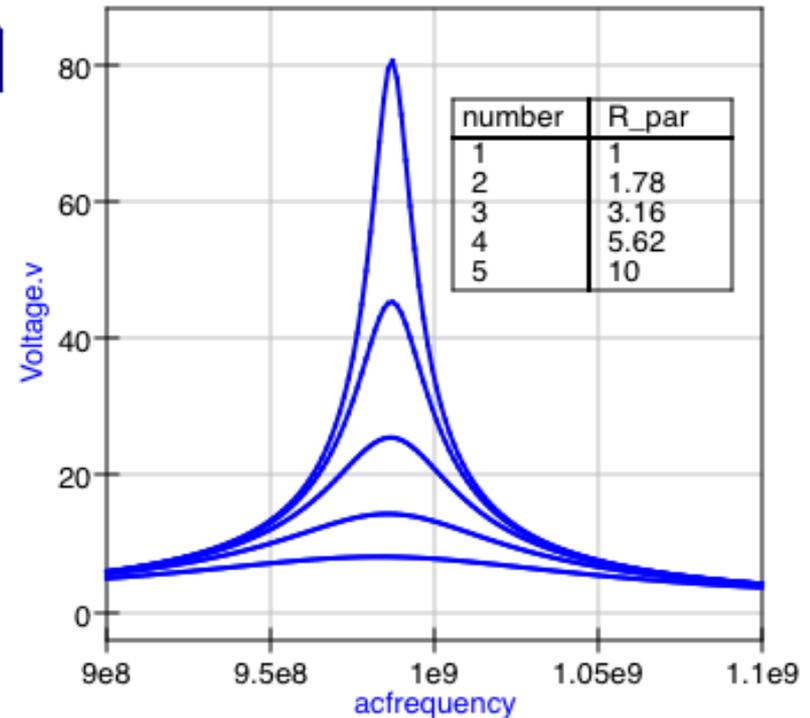
The voltage overshoot strongly depends on the quality of the resonance circuit.

ac simulation

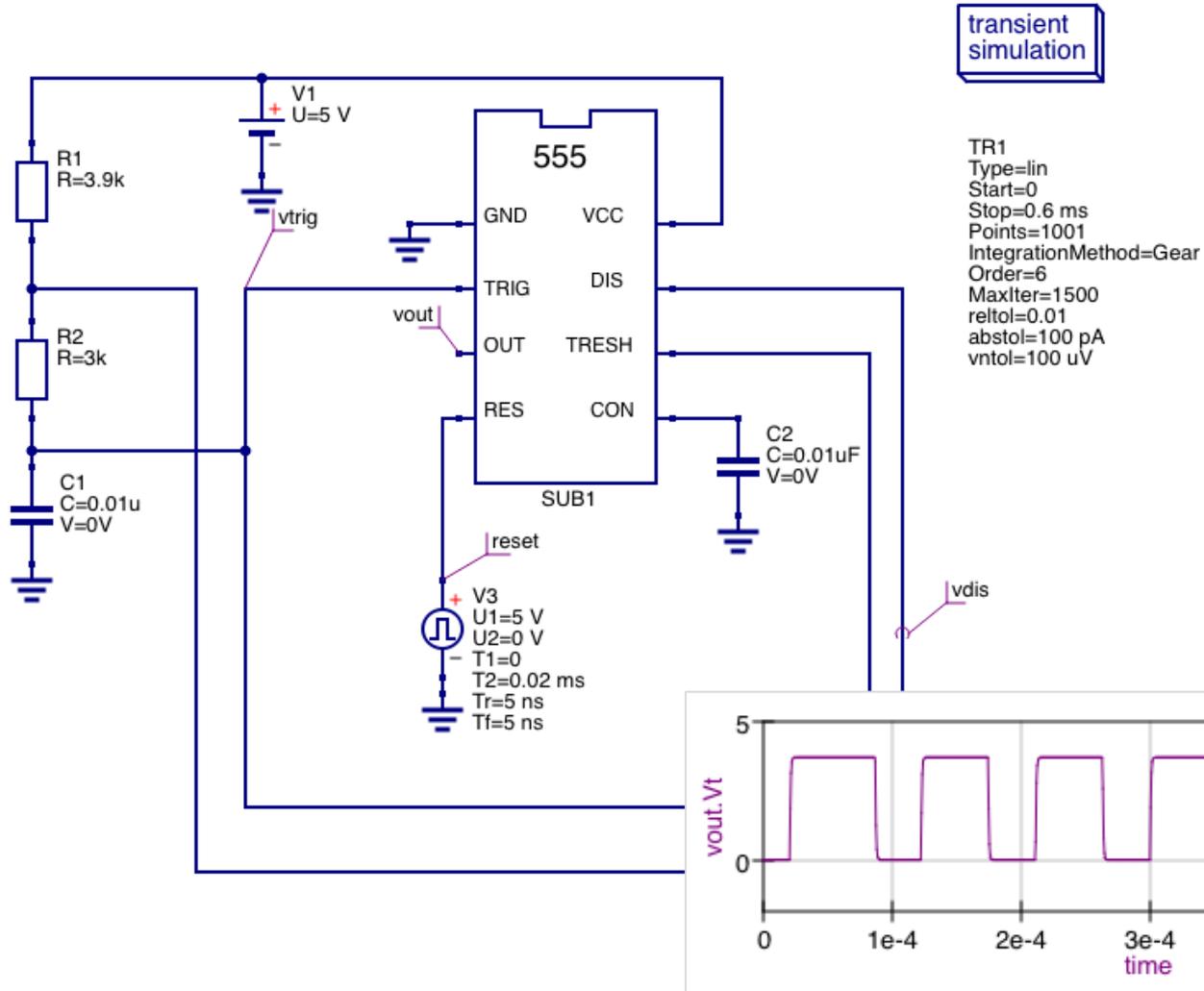
AC1
Type=lin
Start=0.9 GHz
Stop=1.1 GHz
Points=150

Parameter sweep

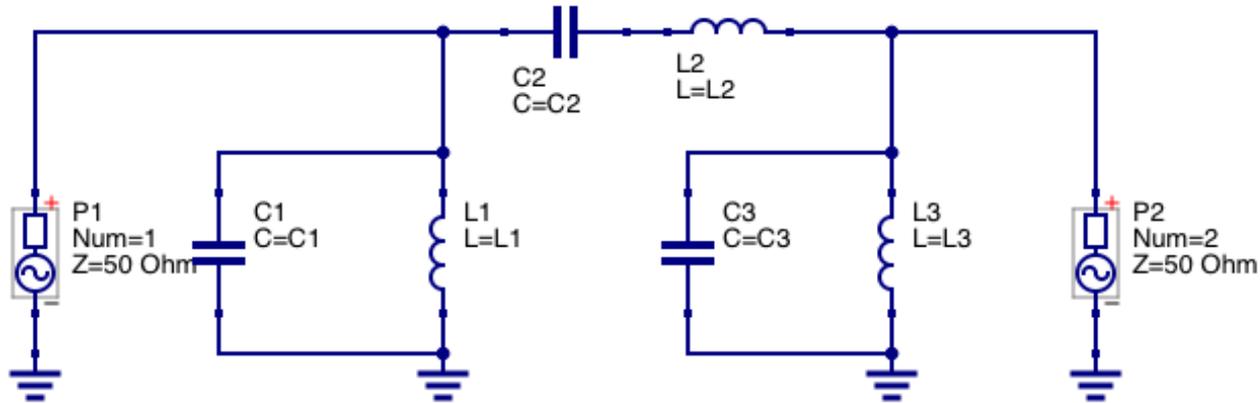
SW1
Sim=AC1
Type=log
Param=R_par
Start=1 Ohm
Stop=10 Ohm
Points=5



555 macro model



Optimization (ASCO)

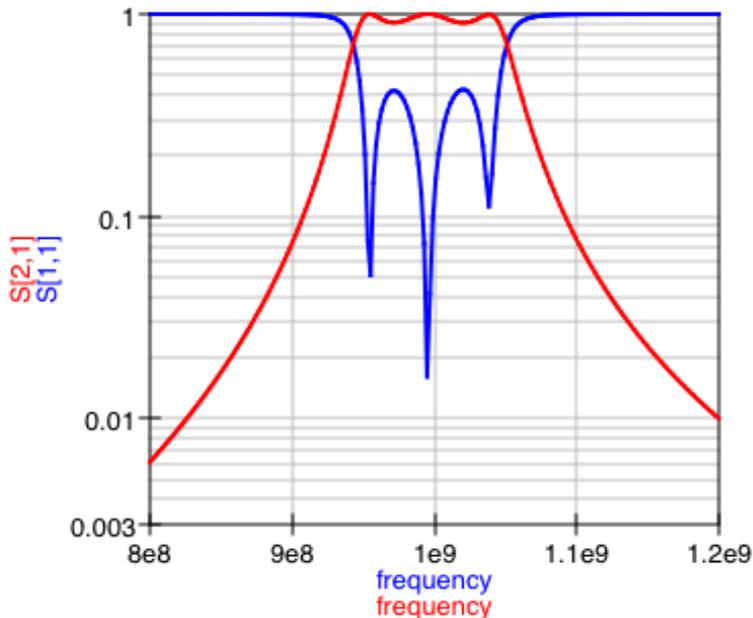


S parameter simulation

SP1
Type=log
Start=800 MHz
Stop=1200 MHz
Points=200

Optimization

Opt1



Equation

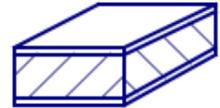
Eqn1
Left_Side_Lobe=max(dB(S[2,1]),800e6:900e6)
Pass_Band_Ripple=min(dB(S[2,1]),960e6:1040e6)
Right_Side_Lobe=max(dB(S[2,1]),1100e6:1200e6)
S11_In_Band=-max(dB(S[1,1]),960e6:1040e6)

number	Left_Side_Lobe	Pass_Band_Ripple	Right_Side_Lobe	S11_In_Band
1	-23.1	-0.856	-22.7	7.47

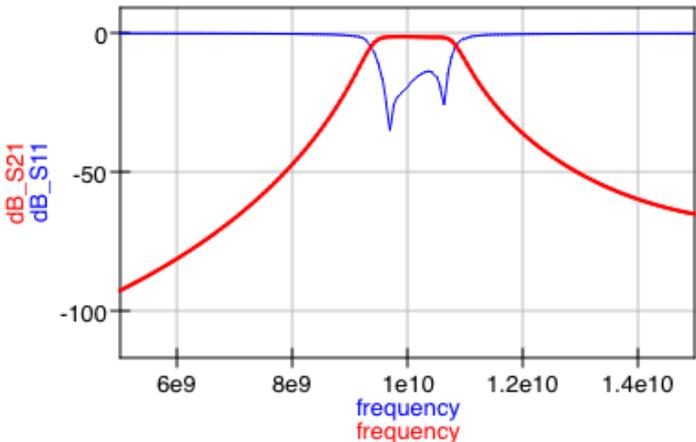
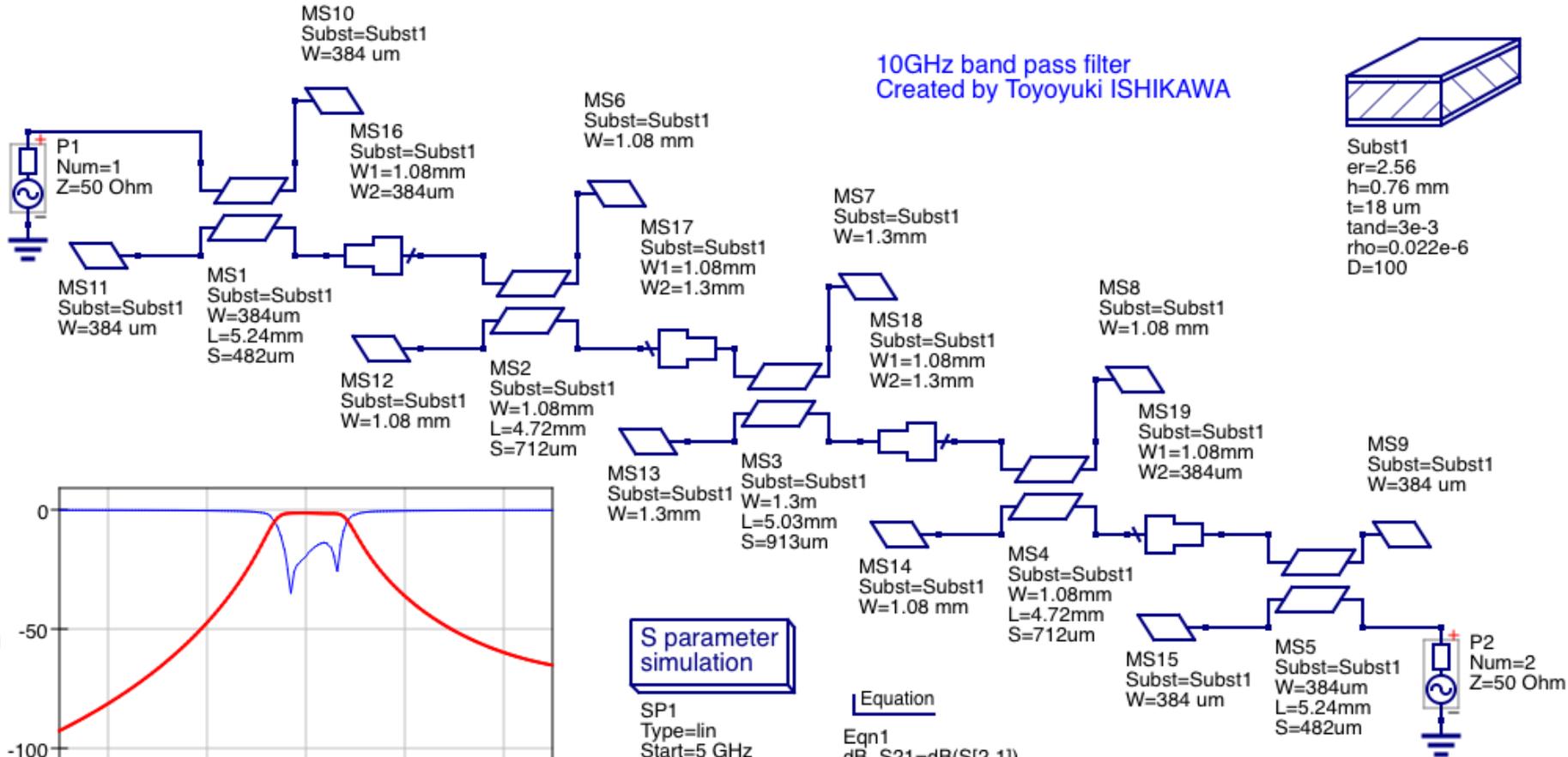


Microstrip band-pass filter

10GHz band pass filter
Created by Toyoyuki ISHIKAWA



Subst1
er=2.56
h=0.76 mm
t=18 um
tand=3e-3
rho=0.022e-6
D=100



S parameter simulation

SP1
Type=lin
Start=5 GHz
Stop=15 GHz
Points=150

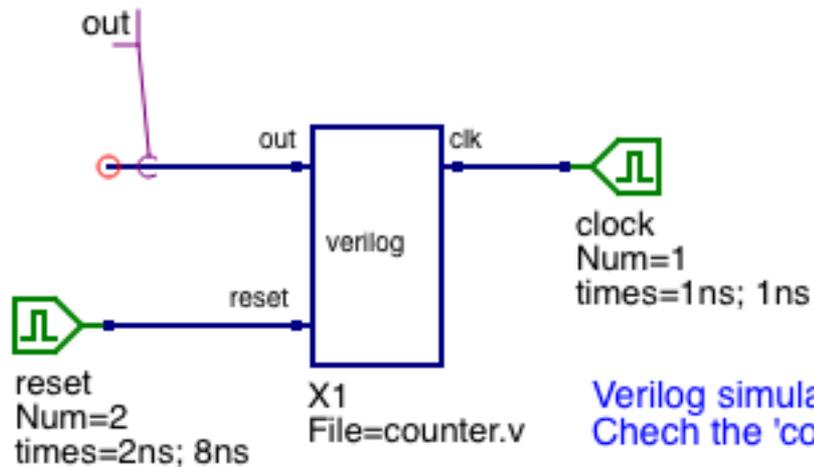
Equation
Eqn1
dB_S21=dB(S[2,1])
dB_S11=dB(S[1,1])



Verilog Counter

digital simulation

Digi1
Type=TimeList
time=10 ns



```
module counter(out, clk, reset);  
  
    parameter WIDTH = 2;  
  
    output [WIDTH-1 : 0] out;  
    input          clk, reset;  
  
    reg [WIDTH-1 : 0] out;  
    wire          clk, reset;  
  
    always @(posedge clk)  
        out <= out + 1;  
  
    always @reset  
        if (reset)  
            assign out = 0;  
        else  
            deassign out;  
  
endmodule // counter
```

Verilog simulation with Icarus Verilog
Check the 'counter.v' for the HDL model.

dtime	0	1n	2n	3n	4n	5n	6n	7n	8n	9n	10n
X1.reset.X	0	1	0	0	0	0	0	0	0	0	1
X1.clk.X	0	1	0	1	0	1	0	1	0	1	0
X1.out.X	00	00	00	01	01	10	10	11	11	00	00



Status

- Release 0.0.19 (January 22, 2017)
 - Bug fixing, usability improvements, build system cleanup
 - Ongoing port Qt3Support to Qt4
 - New active-filter synthesis tool
 - Integration of regression tests
 - Removal of non-GPL models
 - Adopted git-flow branching model
 - 168 issues closed
- Develop (Release 0.0.20)
 - RF and Microwave
 - Tuner
 - Removal of qucs-editor and qucs-help
 - ... (quick release)



Resources

- Website: <http://qucs.sourceforge.net/>
- GitHub (preferred): <https://github.com/Qucs/qucs/>
- SourceForge: <http://sourceforge.net/p/qucs/git/>
- Mailing lists: <http://sourceforge.net/p/qucs/mailman/>
- IRC channel: #qucs
- Forum: <http://sourceforge.net/p/qucs/discussion/>
- Bug trackers:
 - <https://github.com/Qucs/qucs/issues>
 - http://sourceforge.net/p/qucs/_list/tickets
- Source code documentation:
 - <http://qucs.github.io/qucs-doxygen/qucs/index.html>
 - <http://qucs.github.io/qucs-doxygen/qucs-core/index.html>
- Downloads: <http://sourceforge.net/projects/qucs/files/>
- (NEW) Qucs-Help: <http://qucs-help.readthedocs.io/>
- (NEW) Transifex translations:
 - <https://www.transifex.com/projects/p/qucs-desktop/>
 - <https://www.transifex.com/projects/p/qucs-help/>



Final remarks

- User friendly
- Advanced components and modeling features
- We are open for collaboration
- Help is welcome