

# Understanding JESD204B

High-speed inter-device data transfers for SDR

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# Introduction

# JESD204 Standard

- Designed as high-speed serial data link between converter (ADC, DAC) and logic device
  - Up to 32 lanes per link
  - Up to 12.5 Gbps (raw) per lane
- Describes data mapping and framing
- Multi-chip synchronization
- Deterministic latency

# Timeline

- 2006: JESD204
  - 1 lane, 3.125Gbps
- 2008: JESD204A
  - Multi-lane, 3.125 Gbps
- 2012: JESD204B
  - Multi-lane, 12.5 Gbps
  - Deterministic latency
    - Subclass 0, 1, 2
  - More flexible clocking scheme

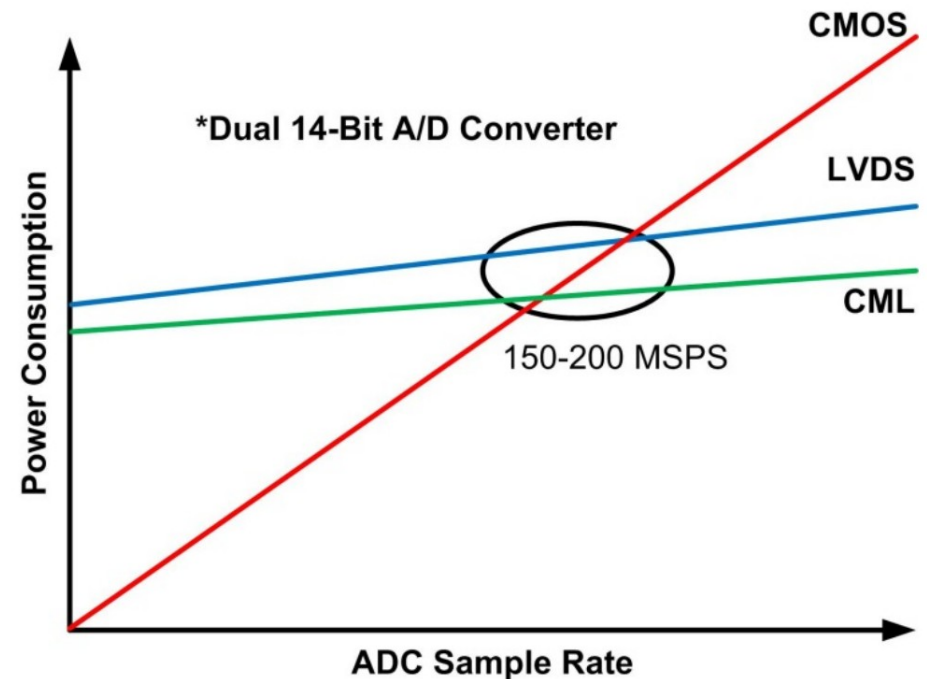
# Motivation

# Increasing Data Demands

- Increasing channel bandwidth
  - 802.11ac: 160 MHz, LTE: 5 \* 20MHz
  - > 1GHz at higher bands
- Diversity transmitter/receiver
  - MIMO, Multi-user
- Direct RF
  - Move parts of the signal chain into the digital domain
  - ADC/DAC directly capture/synthesize RF data

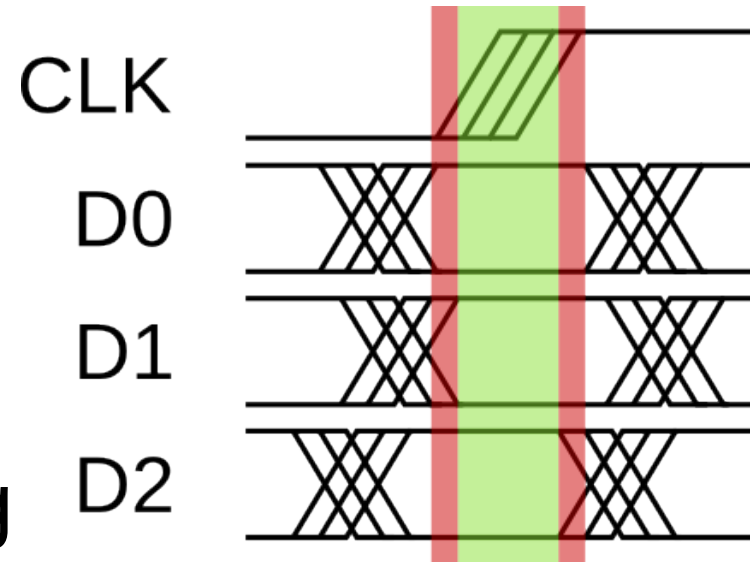
# Replacing Parallel Buses

- To increase throughput on a parallel bus either increase
  - Number of pins
  - Clock rate
- More pins:
  - Routing issues
  - Power concerns



# Jitter on Parallel Buses

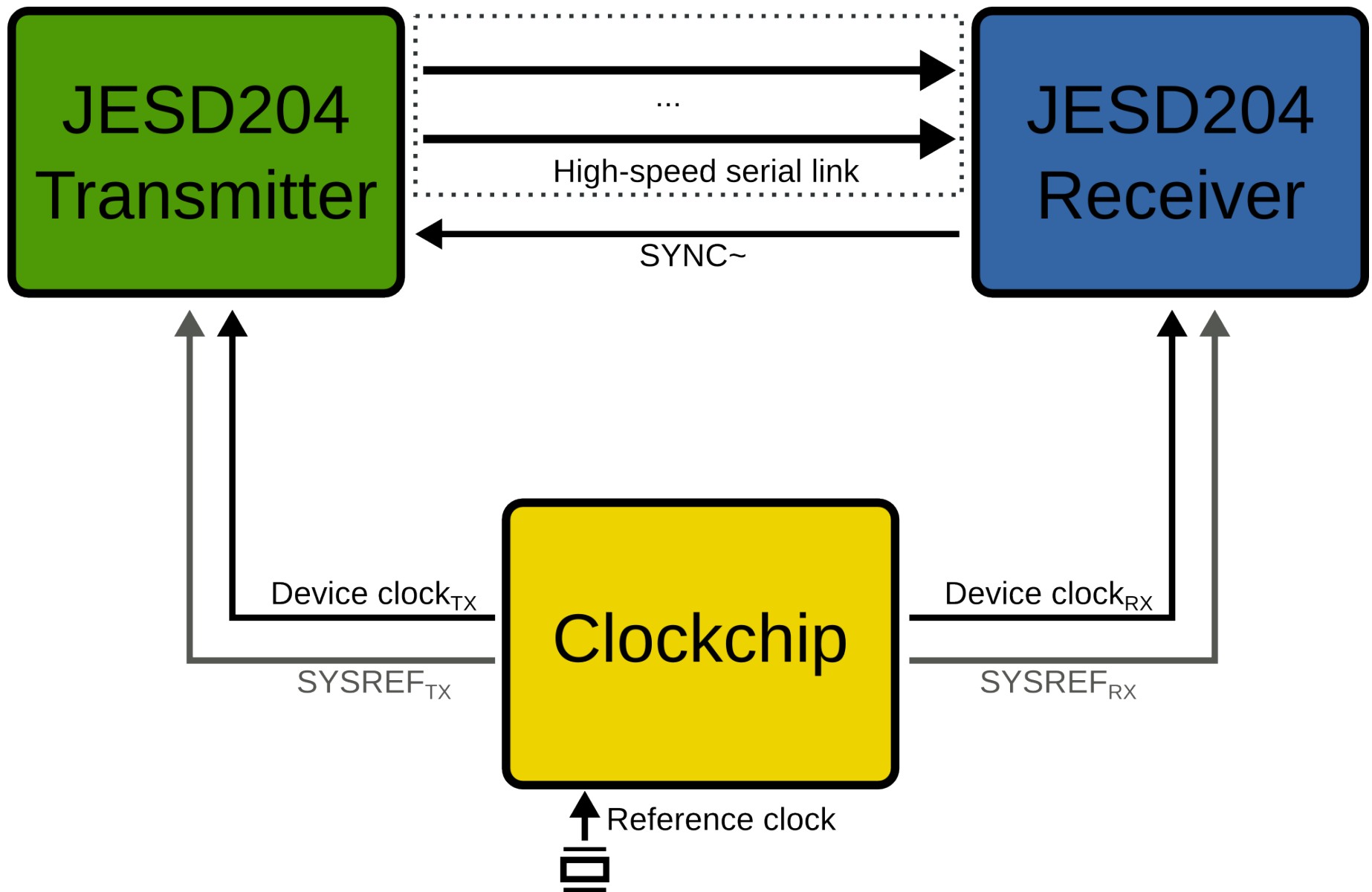
- A parallel bus needs to capture all data lines at the same time
- Complicated by skew and jitter caused by manufacturing and environmental differences
  - Process, Voltage, Temperature (PVT)





# Architecture

# Overview



# Layers

Application

Application specific processing

Transport

Sample framing  
Lane mapping

Link

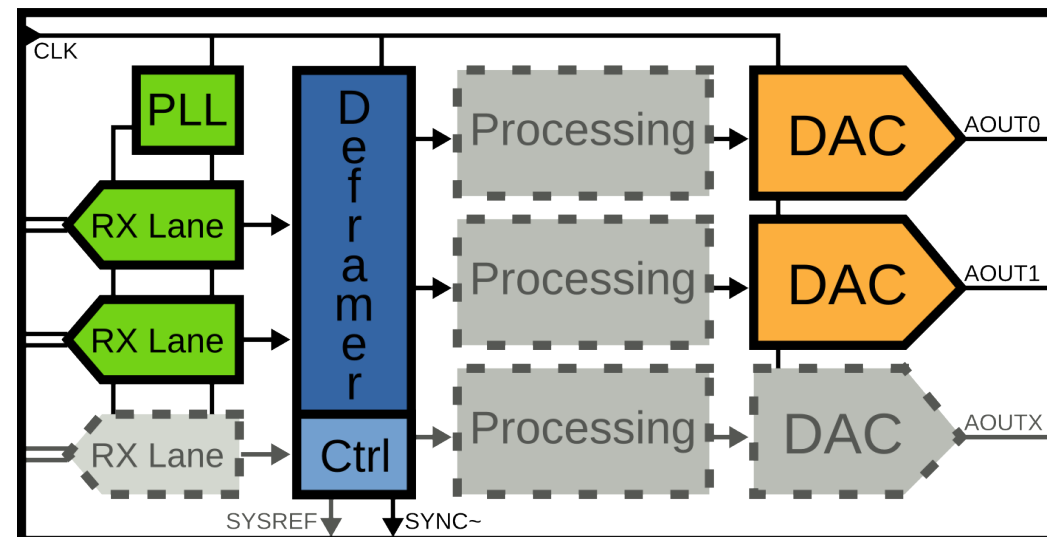
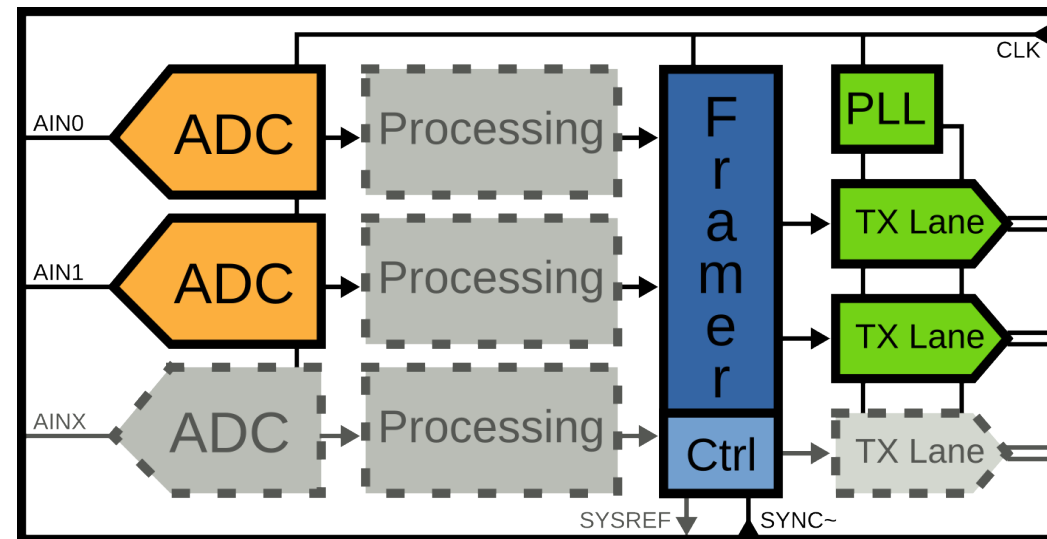
Scrambling  
Character replacement  
8b/10b encoding

Physical

High-speed SerDes  
Clock recovery  
Signal shaping

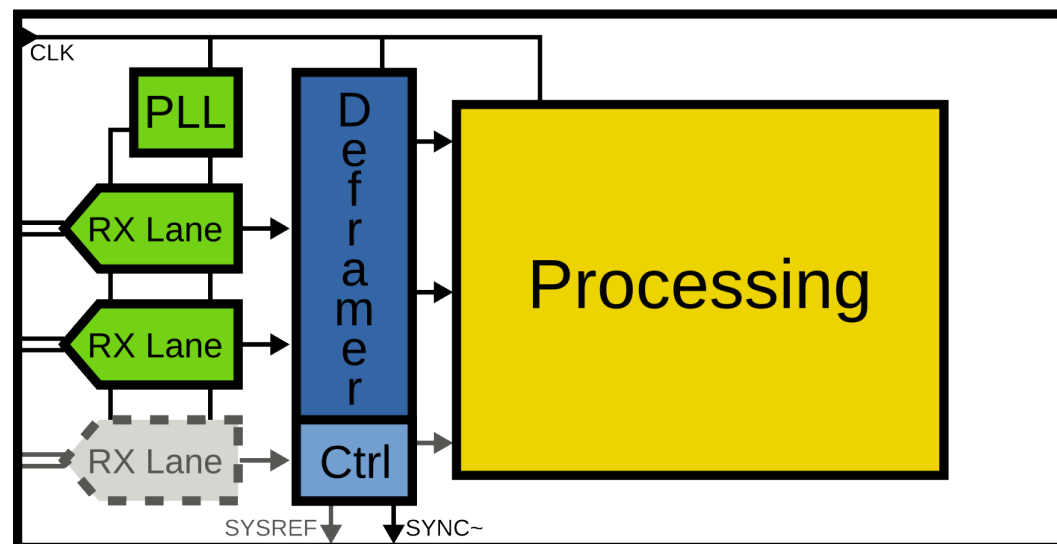
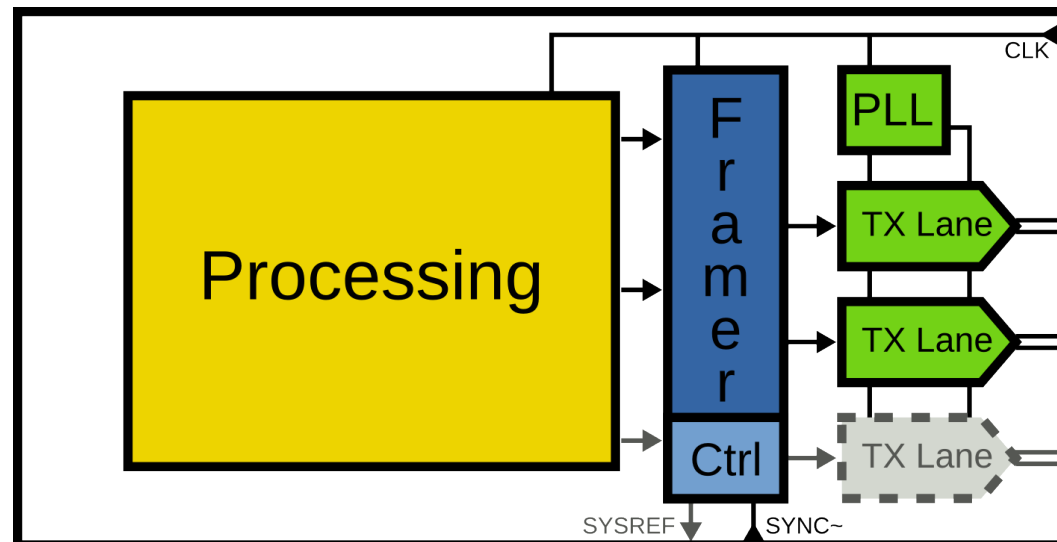
# Converter Device

- Does either A2D or D2A conversion
- Contains one or more converters
  - All synchronous
- Modern converter devices often include digital processing



# Logic Device

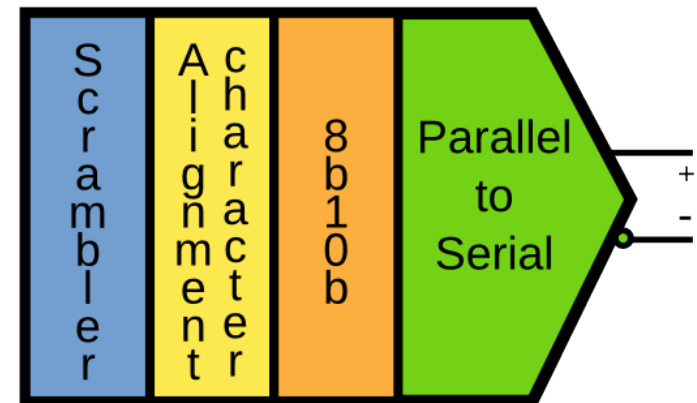
- Implements digital signal processing
- Often implemented in a FPGA
- One logic device can interface multiple synchronous converter devices
  - Multi-point link



# Link

- Link consist of multiple independent lanes
- Differential current-mode-logic (CML) signaling
- 8b/10b data encoding
- Embedded clock
- Data scrambling
  - Optional, but highly recommended

## TX Lane



## RX Lane



# Link/Lane Parameters

- Parameters are used to describe the link and lane configuration

Parameter*	Description
DID	Device identification
LID	Lane identification
F	Octets per frame
K	Frames per multi-frame
L	Number of lanes per converter device
N	Converter resolution
N'	Number of bits per sample (recommended to be multiple of 4)
SCR	Scrambling enabled/disabled
HD	High-density (Single sample split over multiple lanes)
JESDV	JESD204 Version (JESD204A, JESD204B)
SUBCLASSV	JESD204B Subclass (0, 1, 2)

\* Table is a excerpt of the most important parameters

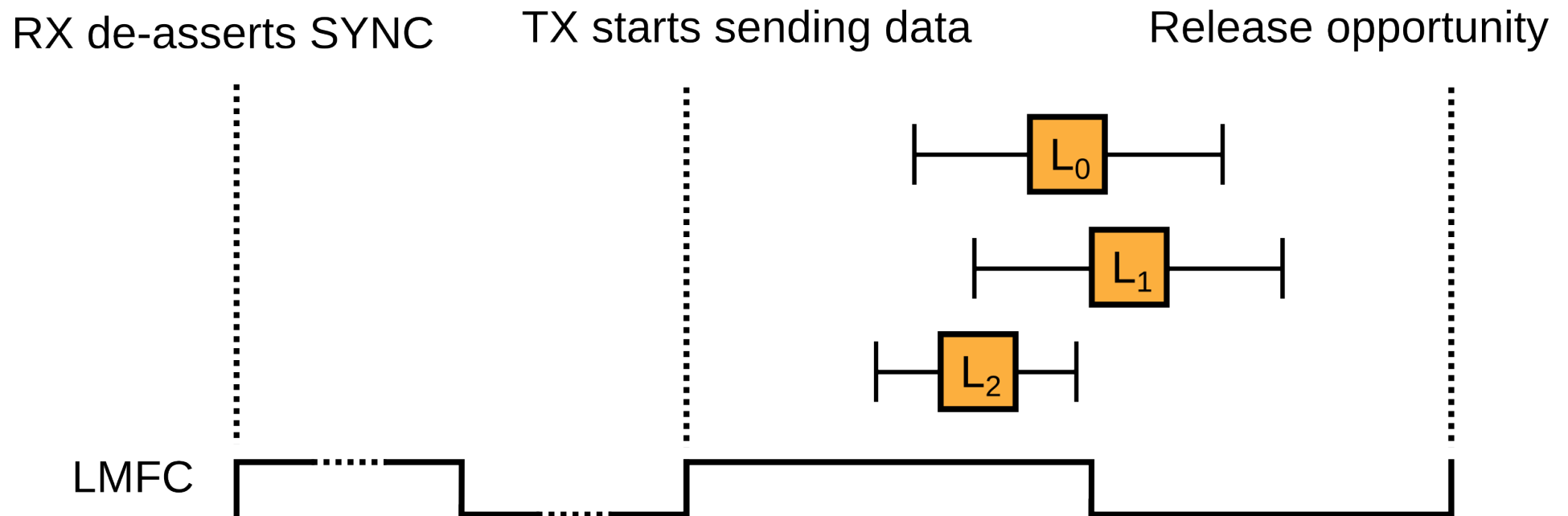
# Deterministic Latency



# Latency

- Propagating data over the link takes time
  - Part of the latency is fixed
  - Part of the latency depends on manufacturing and environmental conditions (PVT)
- Some systems/algorithms are latency sensitive
  - Closed-loop-control systems
  - Radar

# Deterministic Latency



# Deterministic Latency

- End-to-End (JESD link) Latency is consistent (and deterministic) across PVT variations and from power-on to power-on
- Non-deterministic latency components are not removed, but compensated
  - Data is buffered before released to the application layer
  - Release happens at deterministic release opportunities
- Supported by JESD204B subclass 1 and 2

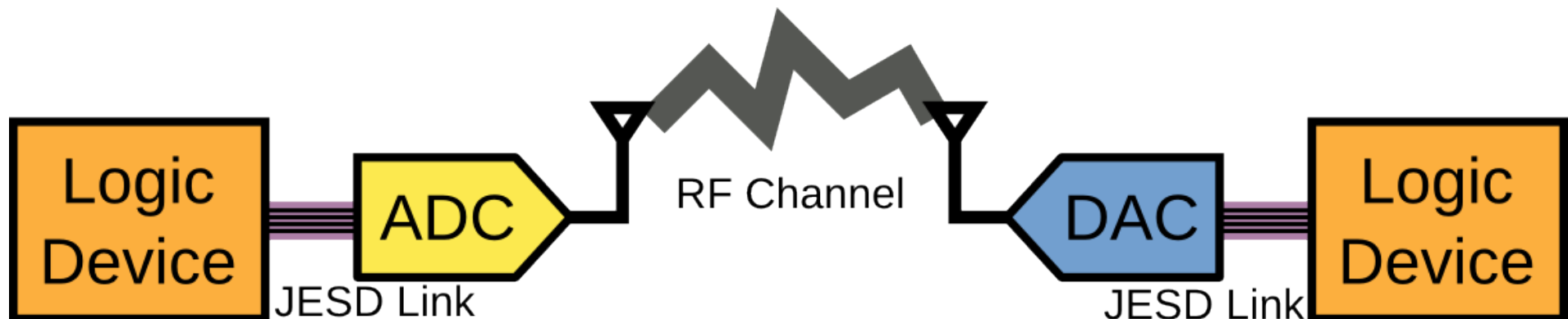
# Data Integrity

# Error Detection

- 8b10b encoding allows detection of simple errors
  - Disparity and not-in-table errors
- Frames with errors should be replaced with the previous frame
  - Most implementations assert an error flag
- No additional data protection
  - No CRC, FEC, etc.

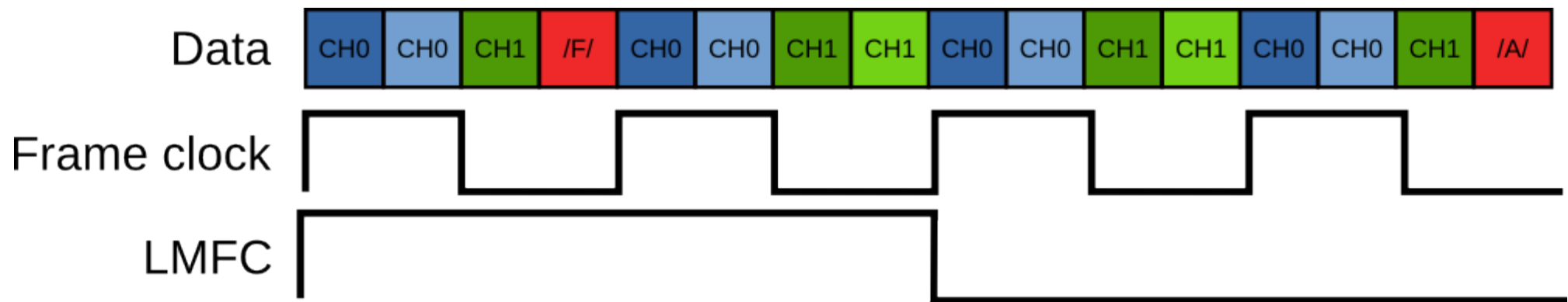
# Data Integrity

- Raw payload data transported over JESD204B link inherently noisy
  - Upper layers implement forward-error-correction and retransmission
- Link bit-error-rate just needs to be good enough



# Alignment Monitoring

- Under certain conditions the last character in a frame/multi-frame is replaced by an alignment control character
  - These control characters will not appear anywhere else in the datastream
  - Allows detection of frame or multi-frame misalignment



# Software Support



# Current Situation

- No common infrastructure
- System integrator has to...
  - research constraints of all system components
  - find one configuration that works for all
  - look-up magic register values for this configuration
- Application developer has to work with provided fixed configuration

# libjesd204 (WIP)

- Built-in database of converter device, logic device and clockchip constraints
  - Programmatic rules establish relationships
    - E.g.  $X = Y / 4$
- System integrator only needs to specify board constraints
  - E.g. number of connected lanes
- Application developer can dynamically change configuration at runtime
  - E.g. set samplerate to 500MSPS
- Configuration automatically mapped to register settings

# Questions and Answers

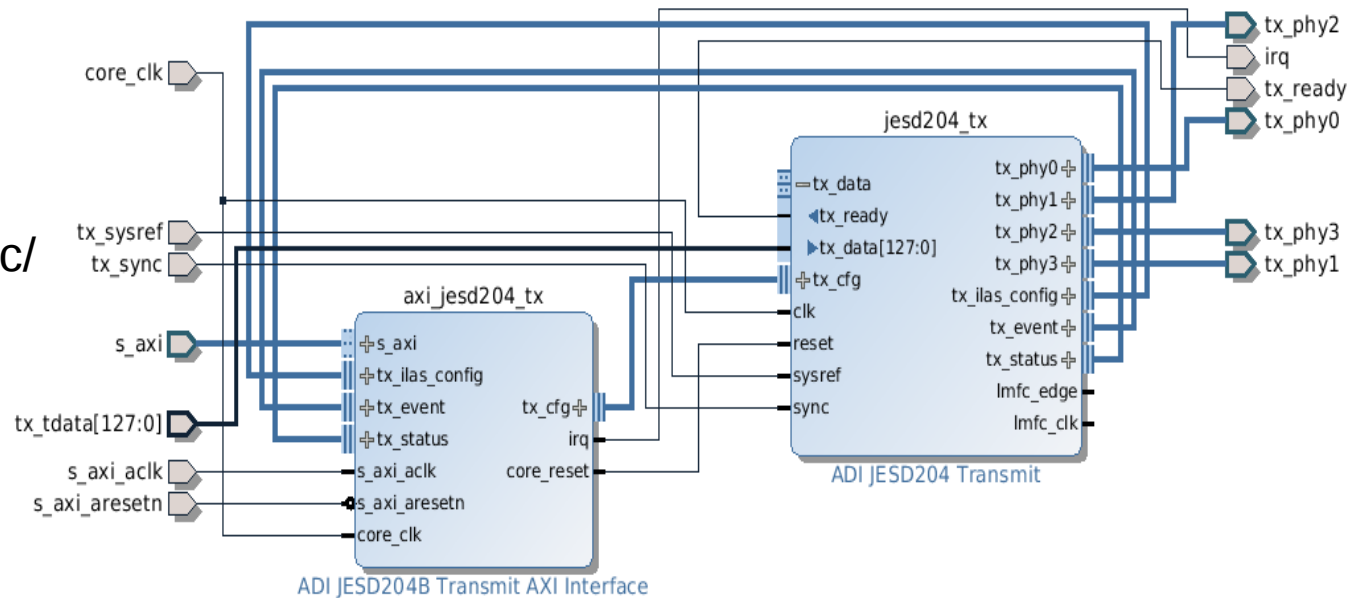
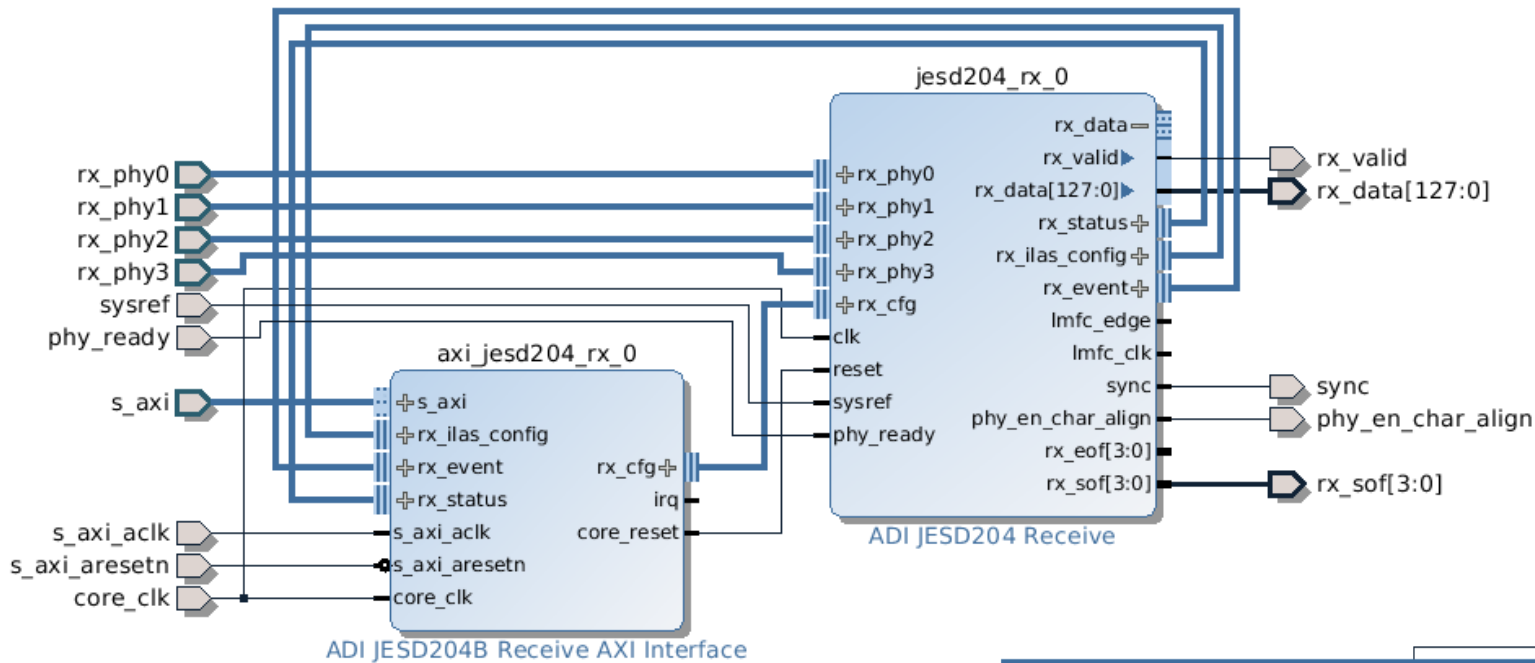
# Additional References

- Analog Devices JESD204B Survival Guide
  - <http://www.analog.com/media/en/technical-documentation/technical-articles/JESD204B-Survival-Guide.pdf>
- M-Labs Open Source JESD204B HDL
  - <https://github.com/m-labs/jesd204b>
- FPGA Vendor JESD204B information:
  - <https://www.altera.com/jesd204b>
  - <https://www.xilinx.com/products/technology/high-speed-serial/jesd204-high-speed-interface.html>

**Thanks**

# Bonus Slides

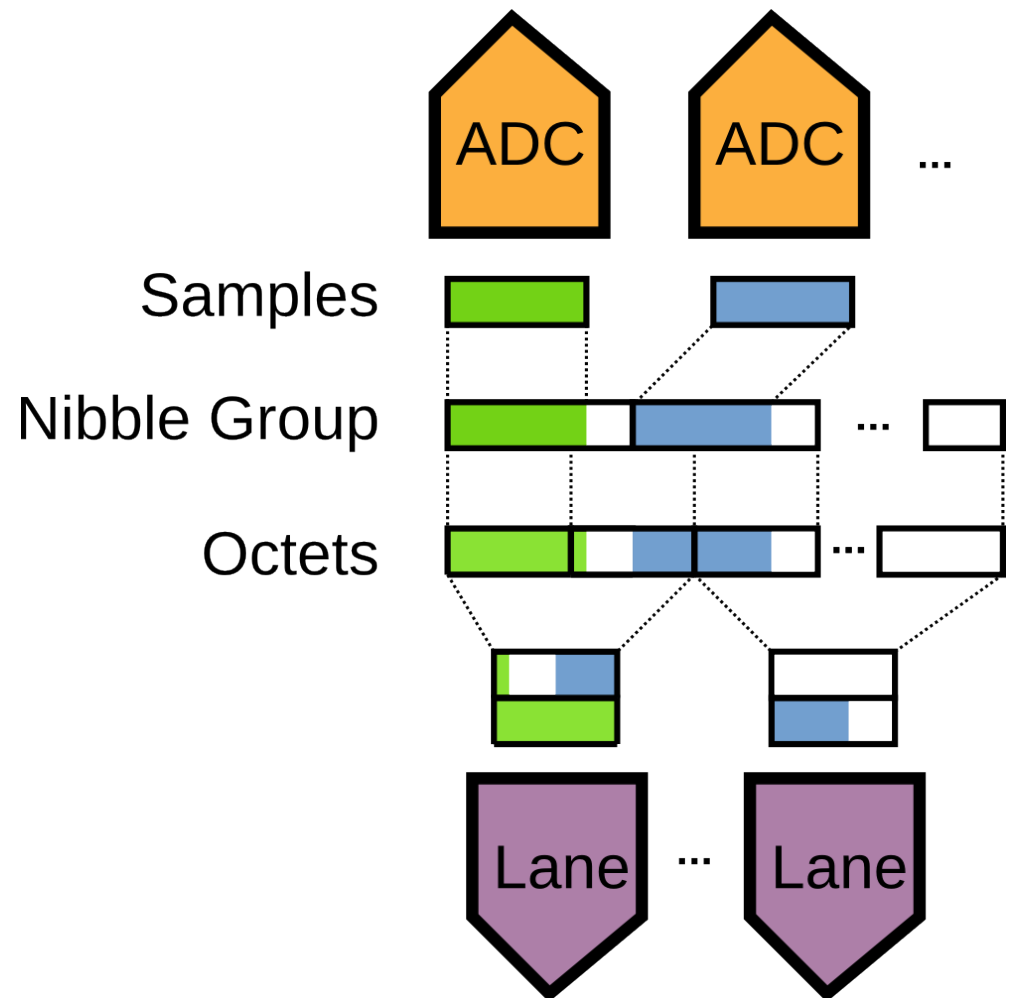
# Available soon



<https://github.com/analogdevicesinc/hdl/tree/dev/library/jesd204>

# Framing

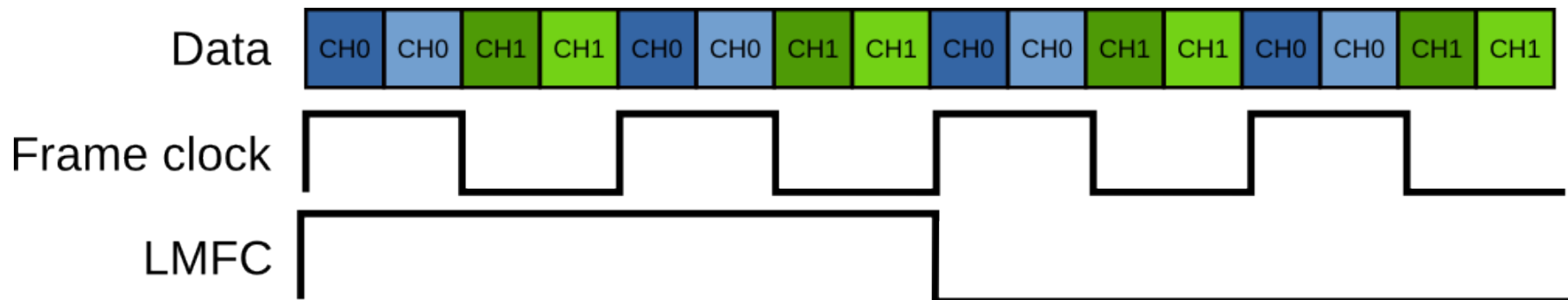
- Samples are mapped into nibble groups
  - Control bits and padding are added
- Nibble groups are mapped to octets
- Octets are processed per lane





# Local Multi-Frame Clock

- Each JESD204B device generates an internal local multi-frame clock (LMFC)
  - 1-32 frames long
- Beginning of the LMFC is synchronized externally
  - Subclass 1: SYSREF, Subclass 2: SYNC
- Internal events are synchronized to the LMFC



# Link Synchronization

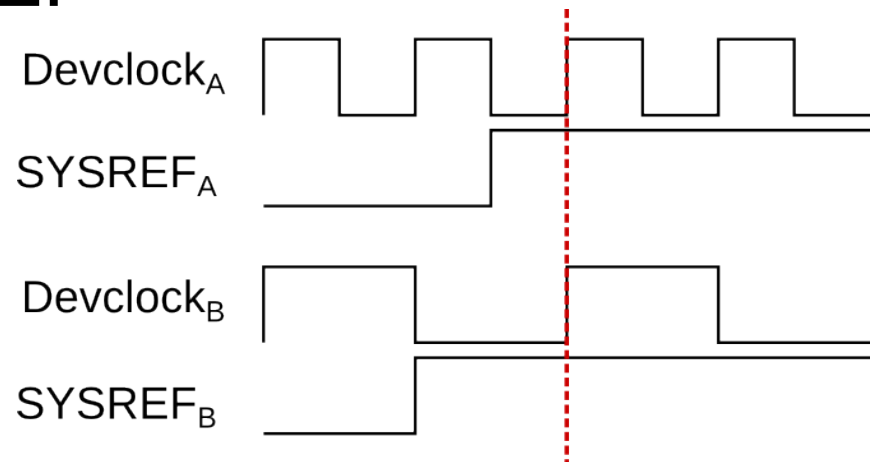
- Receiver asserts SYNC
- Transmitter repeatedly sends /K/ character
- Receiver performs CDC and character alignment
- Receiver de-asserts SYNC
- Transmitter starts sending ILAS and data

# Initial Lane Alignment Sequence

- After link synchronization the transmitter sends the (Initial Lane Alignment Sequence) ILAS
- Allows verification of link alignment
  - Special control character at the start and end of ILAS multi-frame
- Second ILAS multi-frame contains link configuration parameters
  - Allows to verify configuration and lane mapping

# SYSREF

- SYSREF is used as a synchronization signal
  - In subclass 1
- Source synchronous to the device clock
- Three modes
  - Periodic, gapped periodic, one-shot
- LMFC is aligned to SYSREF



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