

Using Red Pitaya for radio applications (from LF to HF)

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Introduction

My journey into radio

– May 2009:

Started to play with FPGA (Altera Cyclone III) and fast ADC (AD9228)

– September 2014:

Discovered RTLSDR, GNU Radio and Gqrx thanks to Hackable Magazine №2

– December 2014:

Started to play with Red Pitaya

– March 2015:

Released Red Pitaya SDR receiver

– September 2015:

Released Red Pitaya SDR transceiver

– November 2015:

Joined Radio & Electronics Engineering Club ASBL (REEC)

Initial goals

- Listen to the radio with ADC and FPGA
- Get familiar with new Xilinx chips and tools
- Keep the number of lines of code low
- Make use of the existing libraries and programs
- Keep the budget low

Red Pitaya

Red Pitaya overview

- A single-board computer designed in Slovenia
- Cost \approx 250 € (tax included)
- Key features:

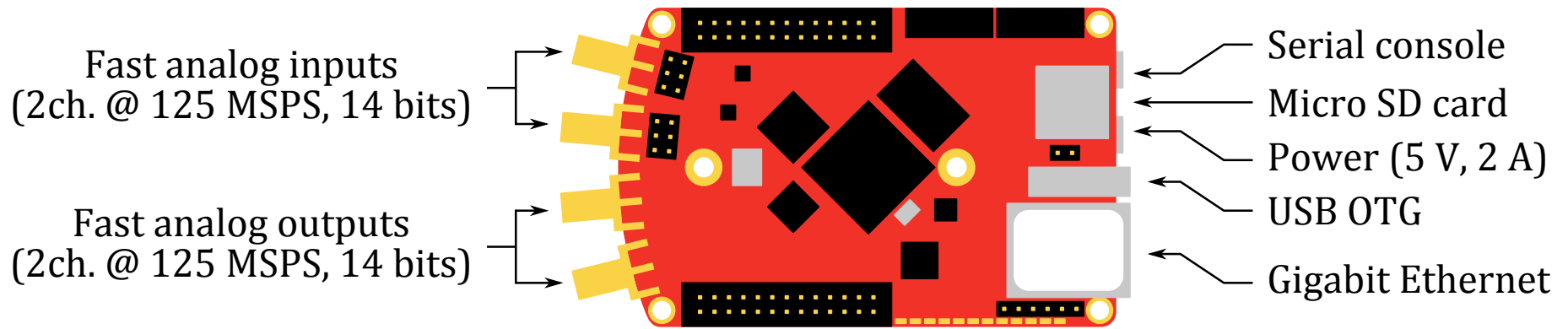
open-source-software measurement and control tool

stand-alone GNU/Linux platform

Xilinx Zynq All Programmable System-on-Chip (ARMv7-A CPU + FPGA)

fast analog inputs and outputs

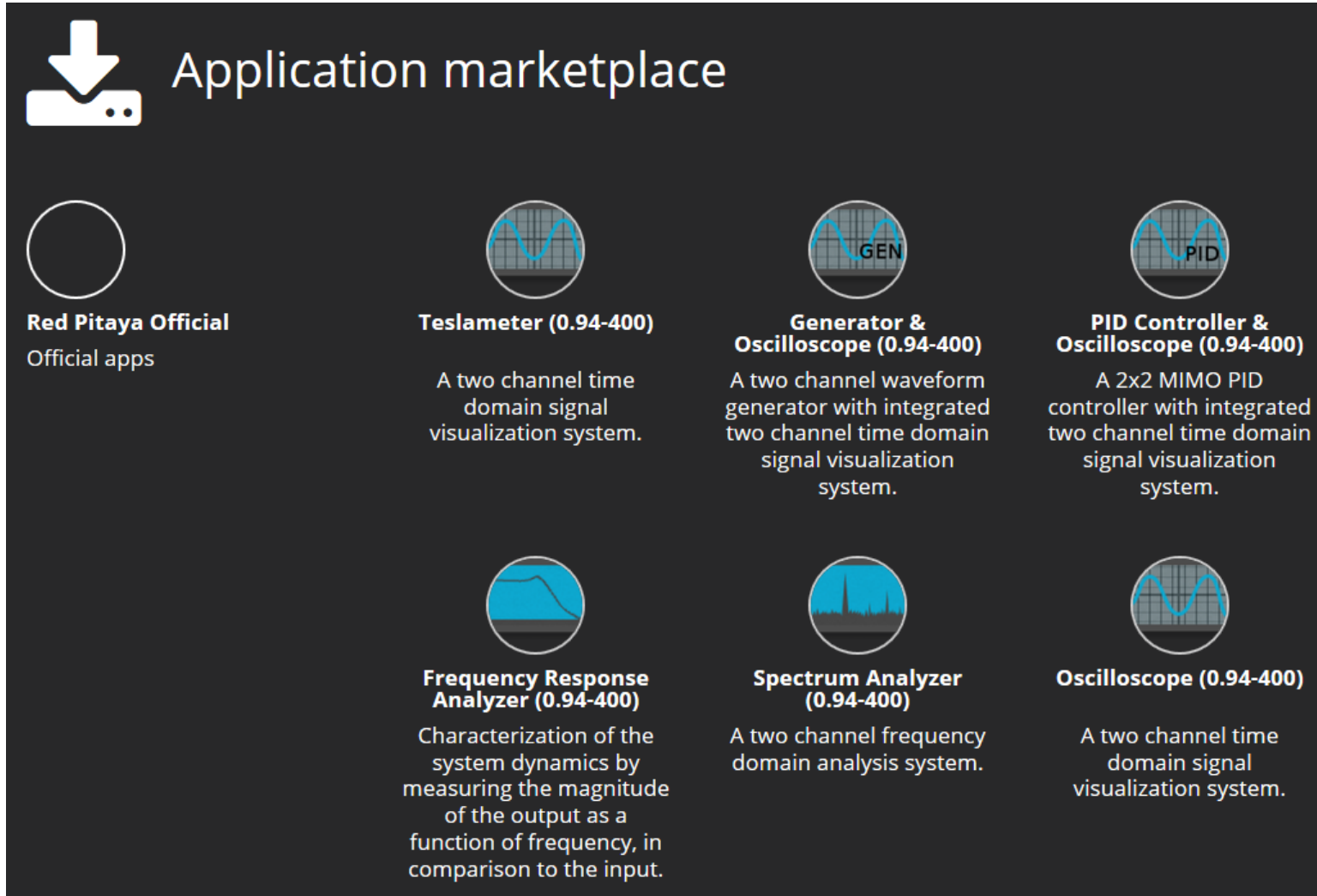
wired and wireless (via a USB adapter) network connectivity



Red Pitaya application marketplace

– Applications can be installed through the application marketplace:

<http://bazaar.redpitaya.com>



The screenshot displays the 'Application marketplace' interface. At the top left, there is a download icon and the title 'Application marketplace'. Below this, there are seven application cards arranged in two rows. Each card features a circular icon representing the application's functionality, followed by the application name and version number, and a brief description of its capabilities.

Application Name (Version)	Description
Red Pitaya Official Official apps	Official apps
Teslameter (0.94-400)	A two channel time domain signal visualization system.
Generator & Oscilloscope (0.94-400)	A two channel waveform generator with integrated two channel time domain signal visualization system.
PID Controller & Oscilloscope (0.94-400)	A 2x2 MIMO PID controller with integrated two channel time domain signal visualization system.
Frequency Response Analyzer (0.94-400)	Characterization of the system dynamics by measuring the magnitude of the output as a function of frequency, in comparison to the input.
Spectrum Analyzer (0.94-400)	A two channel frequency domain analysis system.
Oscilloscope (0.94-400)	A two channel time domain signal visualization system.

Availability

– Its network of distributors makes Red Pitaya easily available worldwide:

LIST OF RED PITAYA DISTRIBUTORS:

Global Authorized Distributor:



EU:



North America:



India:



China:



Asia & Pacific:



South Korea:



Fast analog inputs and outputs

– RF inputs:

Bandwidth: 50 MHz (3 dB)

Input impedance: 1 M Ω // 10 pF

Full scale voltage: 2 V_{pp}

Linear Technology LTC2145-14 ADC:

- two channels, 14 bits, 125 MSPS
- 90 dB SFDR, 73.1 dB SNR, 11.9 ENOB

– RF outputs:

Bandwidth: 50 MHz (3 dB)

Load impedance: 50 Ω

Full scale power: > 9 dBm

NXP DAC1401D125 DAC:

- two channels, 14 bits, 125 MSPS
- 92 dB SFDR

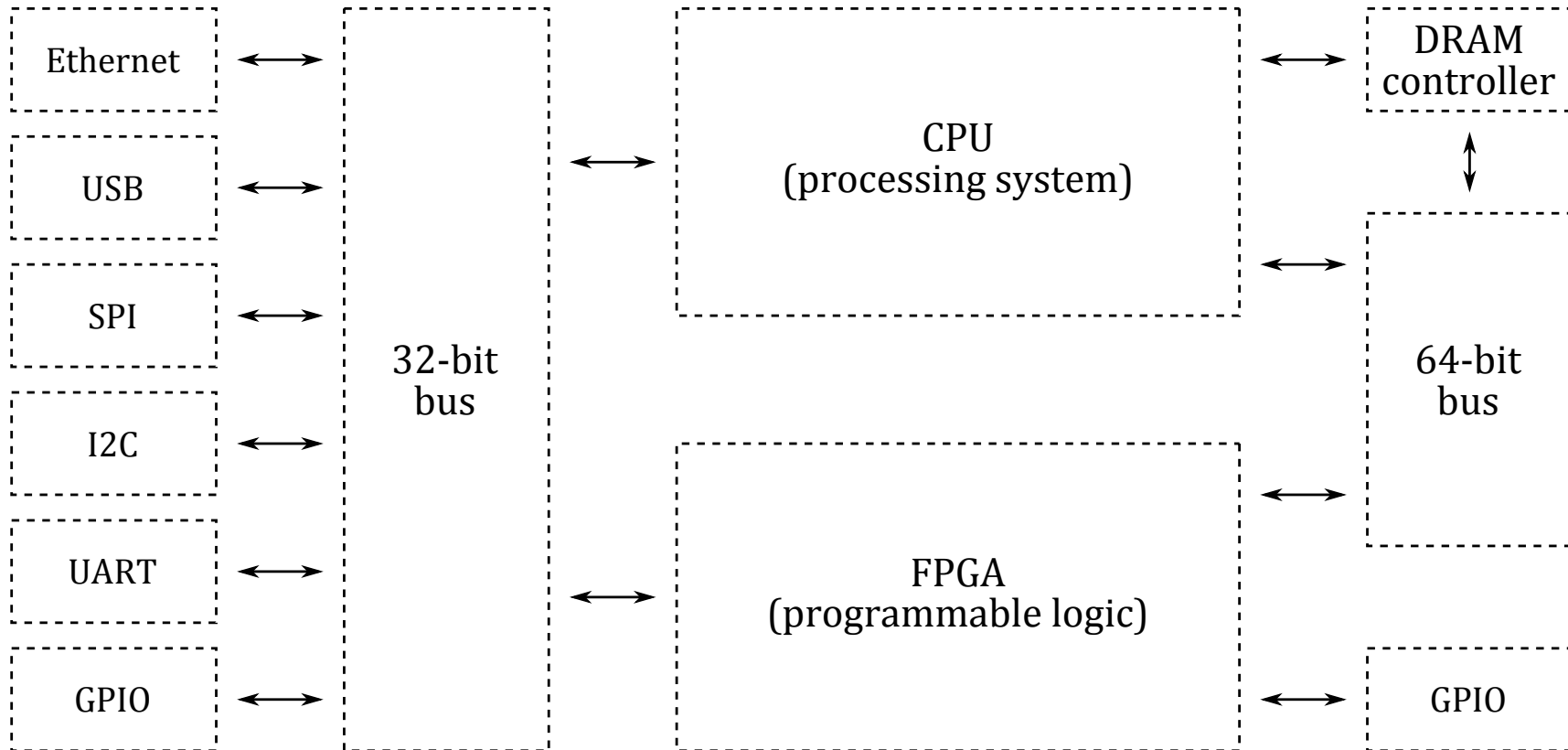
CPU, FPGA and DRAM

- Xilinx Zynq Z-7010 All Programmable System-on-Chip (AP SoC):

CPU: Dual-core ARM Cortex-A9, 667 MHz

FPGA: 2200 logic blocks (CLB), 80 DSP blocks, 60 RAM blocks

- On-board DRAM: 512 MB, DDR3, 1066 MHz, 16-bit wide



FPGA components

- 2200 configurable logic block (CLB):

 - 8× 6-input look-up tables (LUT)

 - 16× flip-flops

- 80 DSP block:

 - 18 × 25 signed multiply

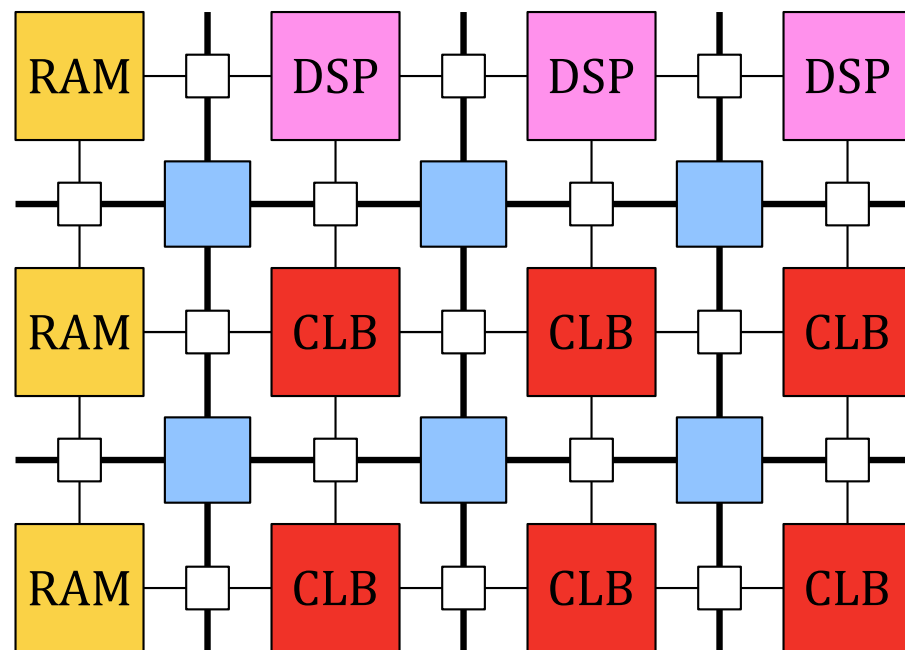
 - 48-bit adder/accumulator

 - 25-bit pre-adder

- 60 RAM block:

 - dual-port

 - 36 Kb

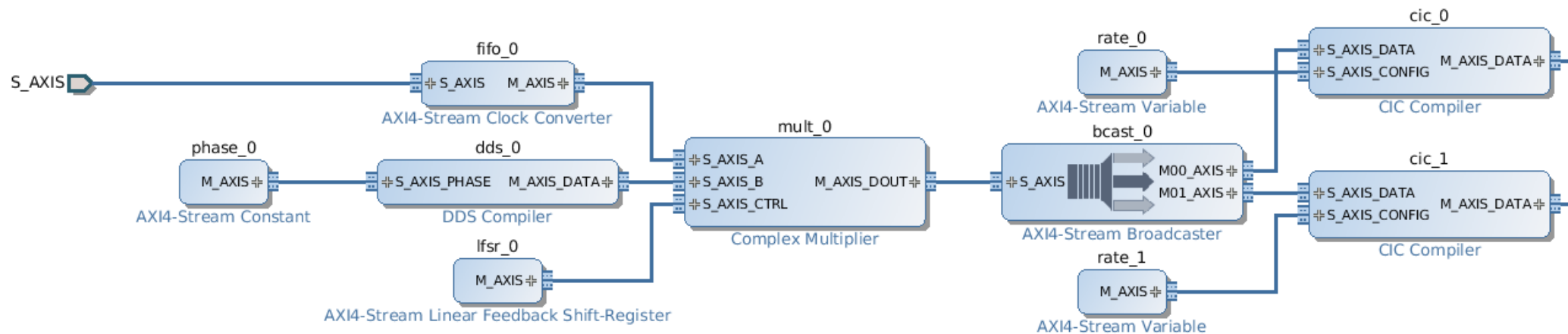


FPGA tools

- Xilinx Vivado Design Suite provides the following tools:
 - Hardware description languages (Verilog and VHDL)
 - Rich library of IP cores (DSP, math, video, imaging, etc)
 - IP Integrator (supports graphical and Tcl-based design flows)
 - High-Level Synthesis for C, C++ and SystemC
- For my projects, I'm currently using:

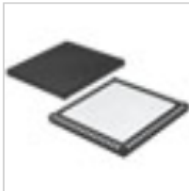
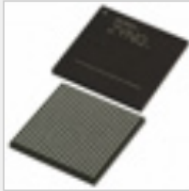


Verilog to write custom IP cores

Tcl to glue IP cores together



Some thoughts about cost

– ADC, AP SoC and SMA connectors are relatively expensive parts:

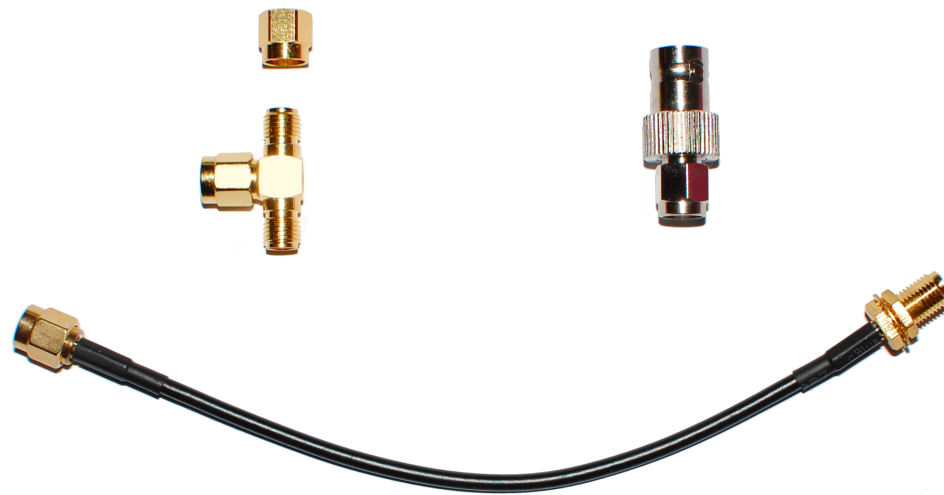
Image	Part Number	Description	Customer Reference	Available Quantity	Backorder Quantity	Unit Price	Extended Price
	LTC2145CUP-14#PBF-ND	IC ADC DUAL 14BIT 125MSPS 64-QFN	LTC2145-14 ADC	1 Immediate	0	68,91000	€ 68,91
	122-1854-ND	IC SOC CORTEX-A9 ARTIX-7 400BGA	Zynq Z-7010 AP SoC	0 Immediate	1 Lead Time	57,43000	€ 57,43
	J502-ND	CONN SMA JACK 50 OHM EDGE MNT	SMA connectors	4 Immediate	0	4,66000	€ 18,64
	1450-1095-ND	IC SDRAM DDR3 256M X 16 96-FBGA	512 MB DDR3 DRAM	1 Immediate	0	8,68000	€ 8,68
						Subtotal	€ 153,66

– Components in small quantities would cost more than the assembled board

Minimal kit for radio applications

1×	Red Pitaya Open Source Instrument	250 €
1×	Fan, 30 × 30 × 15 mm, 5 V	15 €
1×	Power supply, micro USB, 5 V, 2 A	10 €
2×	SMA tee adapter, SMA plug, SMA jack, SMA jack	35 €
2×	SMA terminator, 50 Ω	10 €
4×	SMA-BNC adapter, SMA plug, BNC jack	25 €
4×	SMA cable, SMA jack, SMA plug, RG-174, 15 cm	15 €

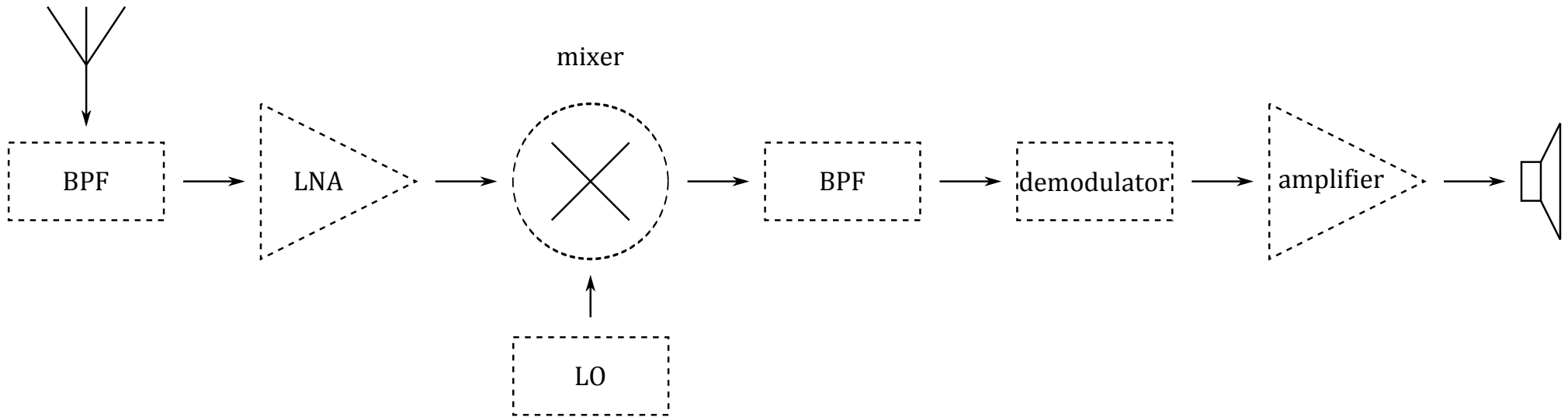
Total 360 € (tax included)



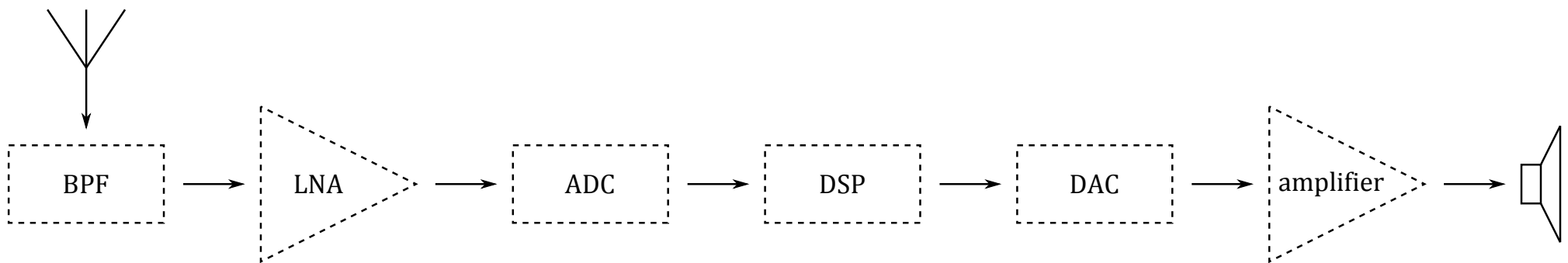
Software defined radio (SDR)

Software defined radio (SDR)

– Superheterodyne receiver:



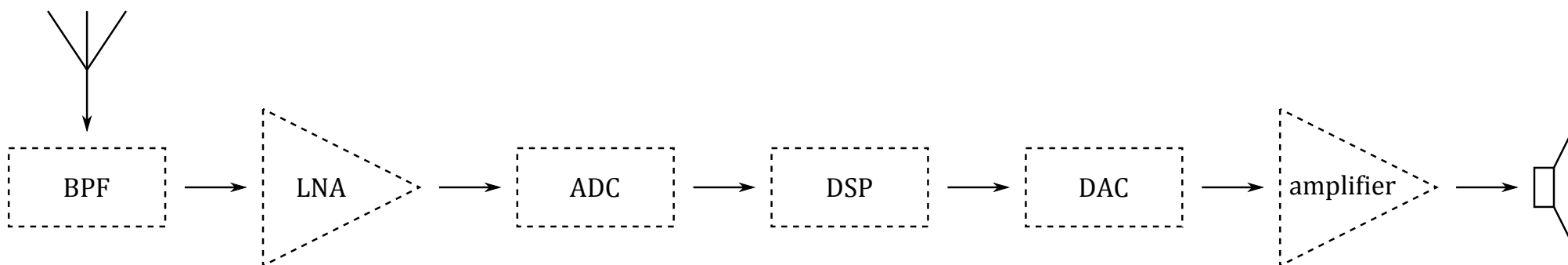
– SDR receiver:



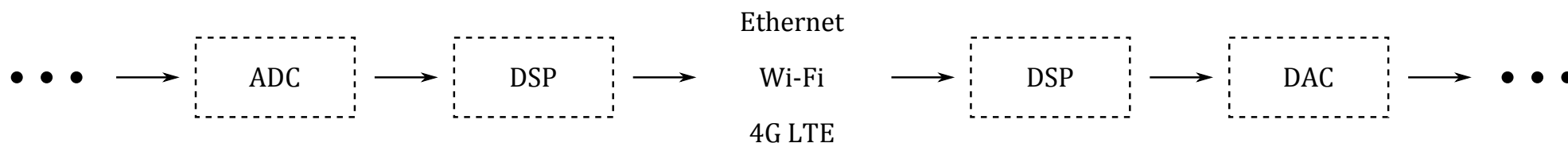
– LO, mixer, filter and demodulator are done by digital signal processing (DSP)

Localized and distributed DSP

– DSP can be localized (e.g. GNU Radio running on the on-board CPU):



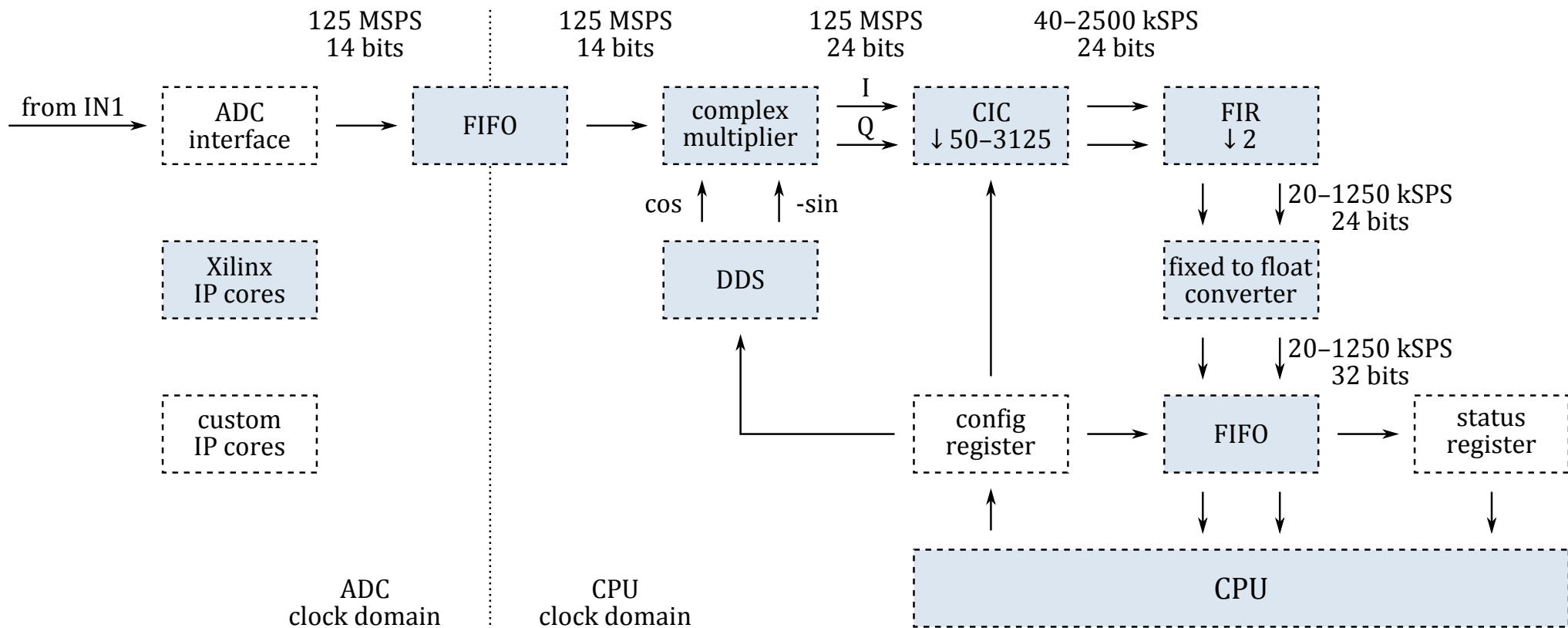
– or distributed:



ADC samples (125 MSPS, 16 bits)	2000 Mb/s
Ethernet	500 Mb/s
Wi-Fi	50 Mb/s
4G LTE	5 Mb/s
Audio (48 kSPS, 16 bits)	1 Mb/s

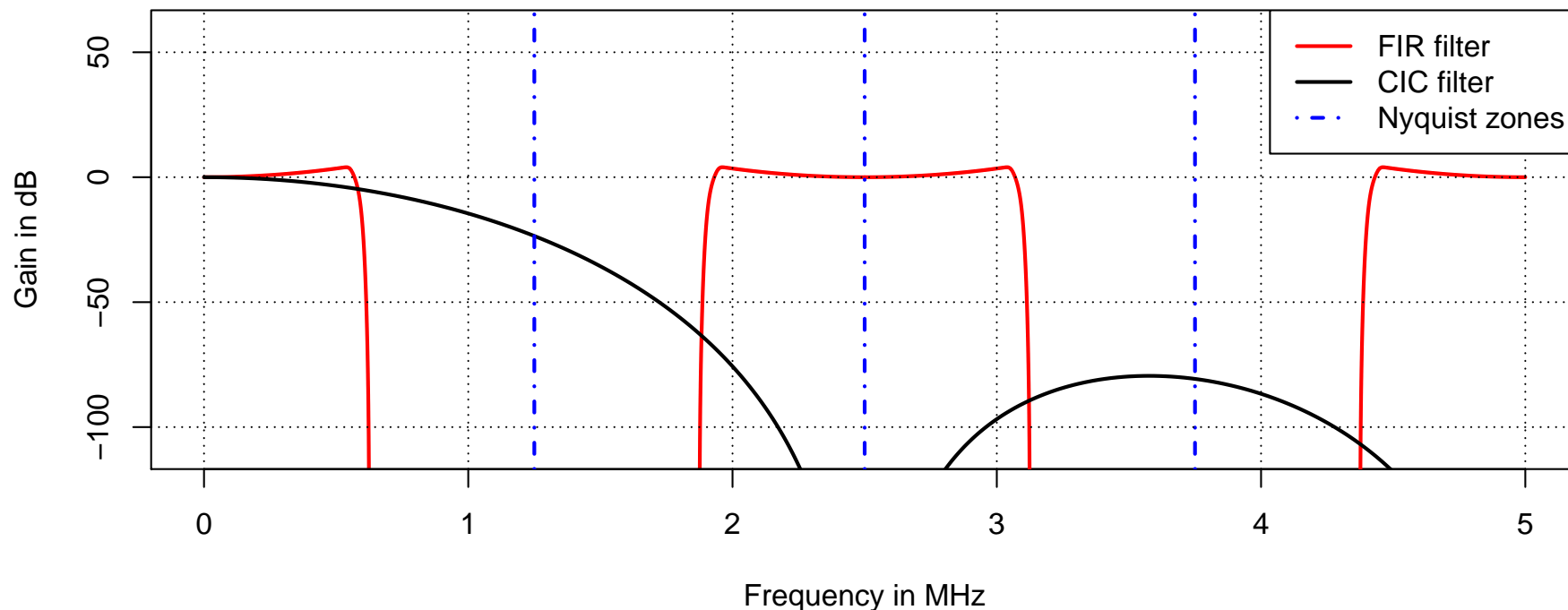
Digital down-converter (DDC)

– ADC samples are processed by a digital down-converter (DDC) running on the Red Pitaya's FPGA:

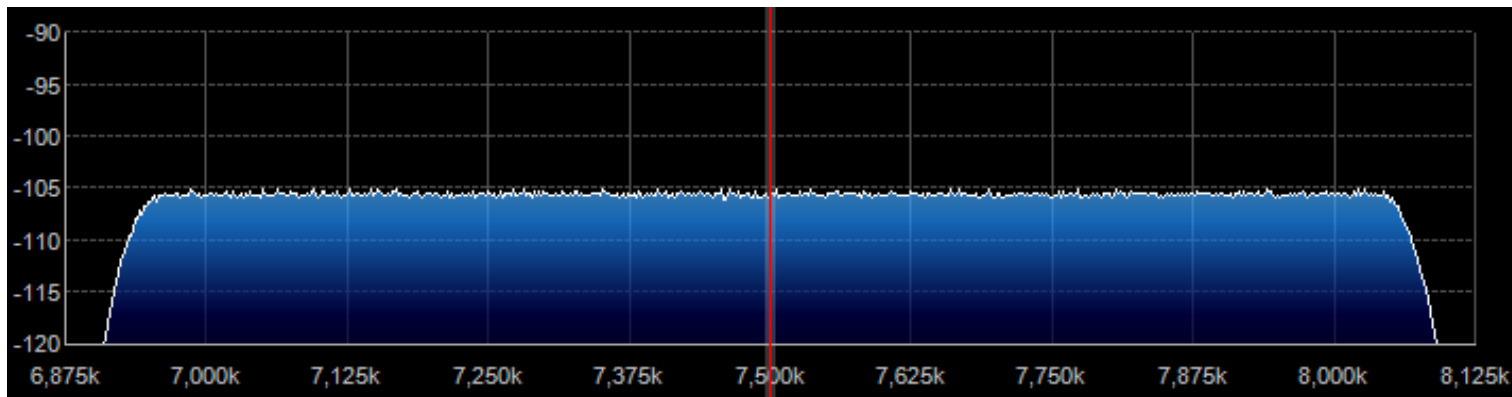


CIC and FIR filters

– Calculated frequency response (decimation by a factor of 50):

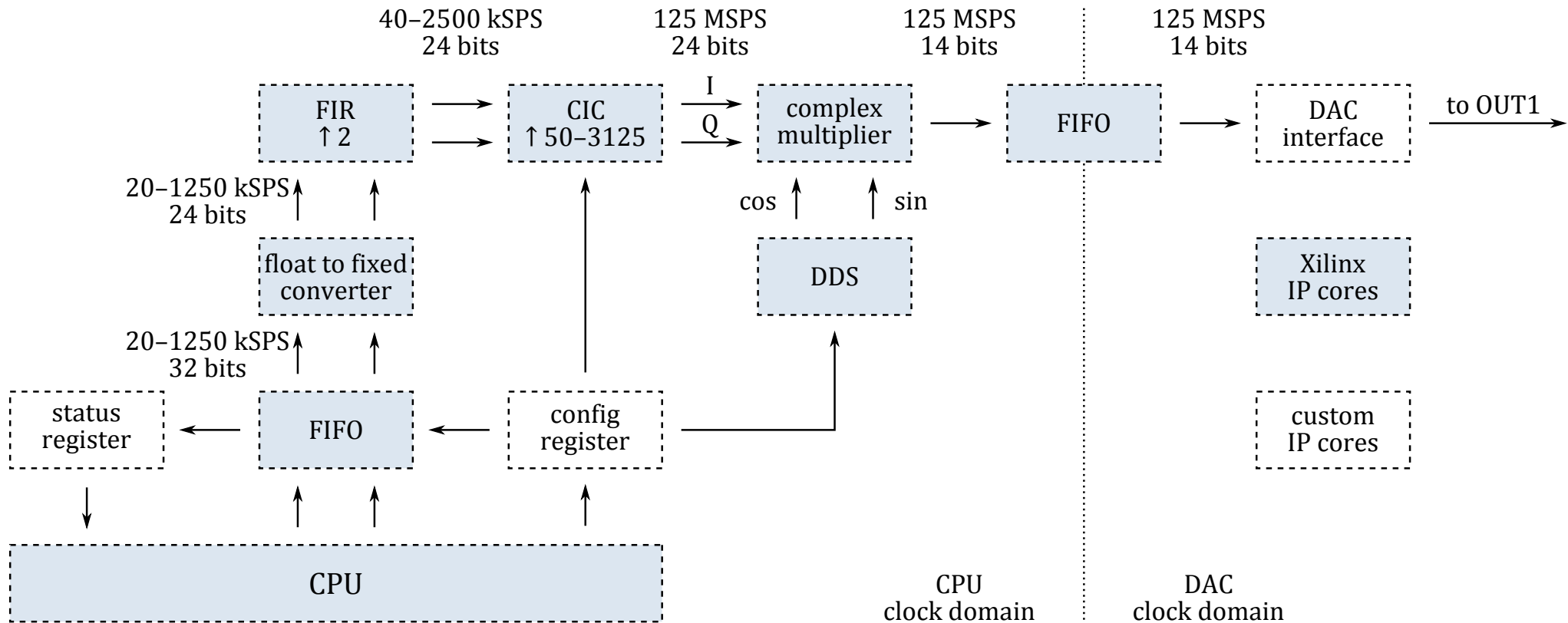


– Measured frequency response:






Digital up-converter (DUC)

– Digital up-converter (DUC) consists of the similar blocks but arranged in an opposite order:

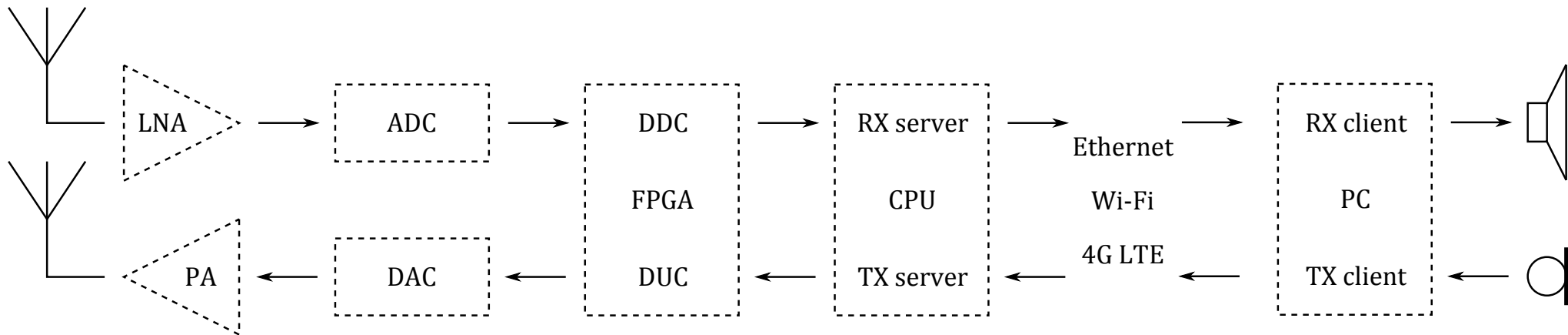


Putting it all together

– Two SDR transceiver applications are available from the Red Pitaya application marketplace:

 Contributed Contributed Apps	 SDR transceiver (0.94-844) Dual channel SDR transceiver compatible with SDR#, HSDR and GNU Radio. (by Pavel Demin)	 SDR transceiver compatible with HPSDR (0.94-861) SDR transceiver emulating a HPSDR transceiver with one network interface module, two receivers and one transmitter. (by Pavel Demin)
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– These applications configure FPGA and start TCP or UDP servers that communicate with SDR programs running on a remote PC:



SDR programs

– SDR programs provide:

graphical user interface

spectrum display

modulation/demodulation

– Red Pitaya SDR transceiver applications work with the following programs:

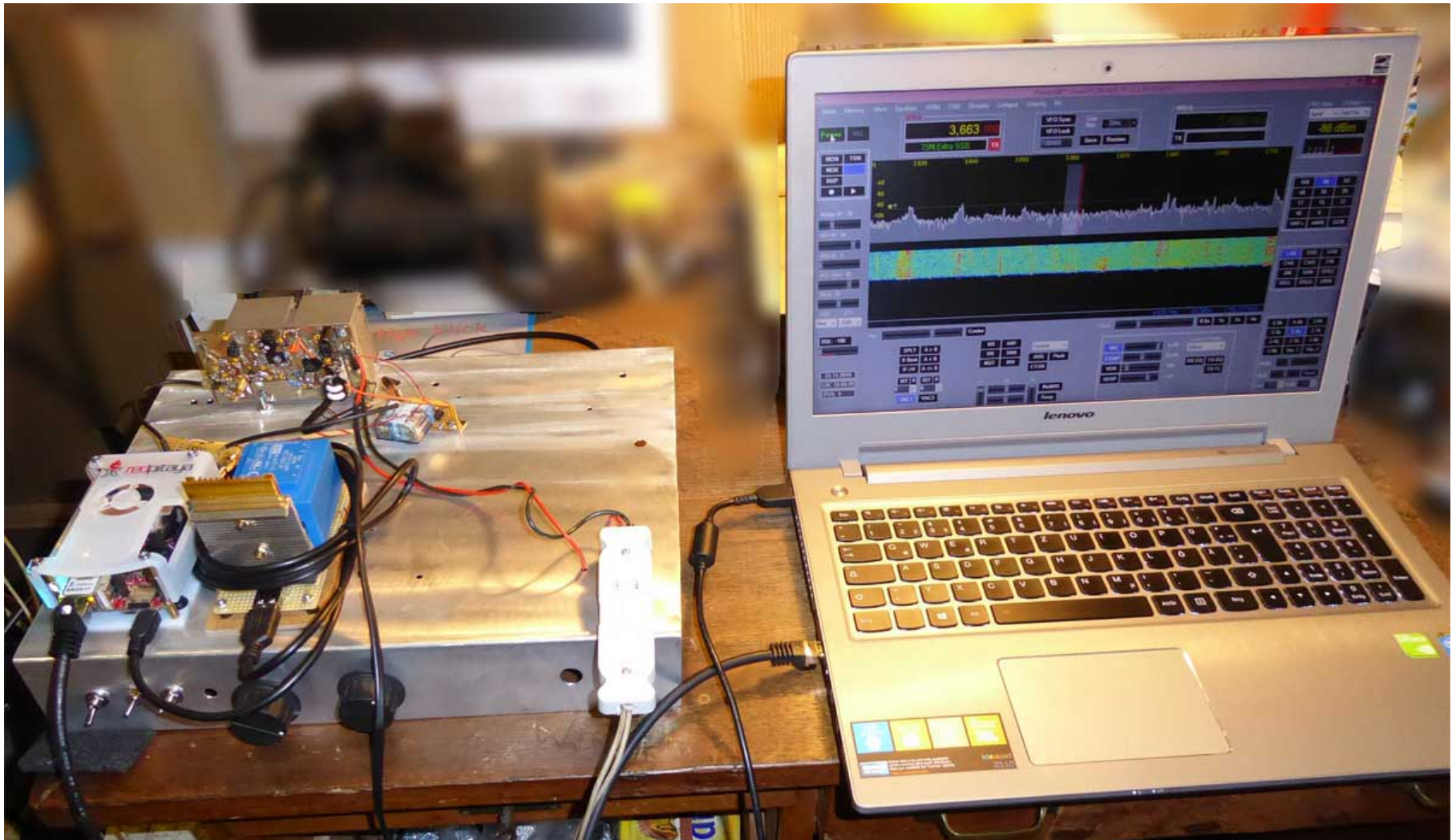
plug-ins/libraries/protocols	SDR programs
ExtIO_RedPitaya_TRX plug-in (only RX)	HDSDR SDR# ($\leq 1.0.0.1361$)
gr-osmosdr/lib/redpitaya	GNU Radio and GNU Radio Companion Gqrx
SoapySDR/SoapyRedPitaya	Pothos CubicSDR
HPSDR/Metis communication protocol	PowerSDR mRX PS QUISK ghpsdr3-alex openHPSDR Android Application Ham VNA vector network analyzer

Feedback from radio amateurs

Red Pitaya SDR with 5W power amplifier

– Wolfgang Kiefer (DH1AKF) published pictures of his 5W station:

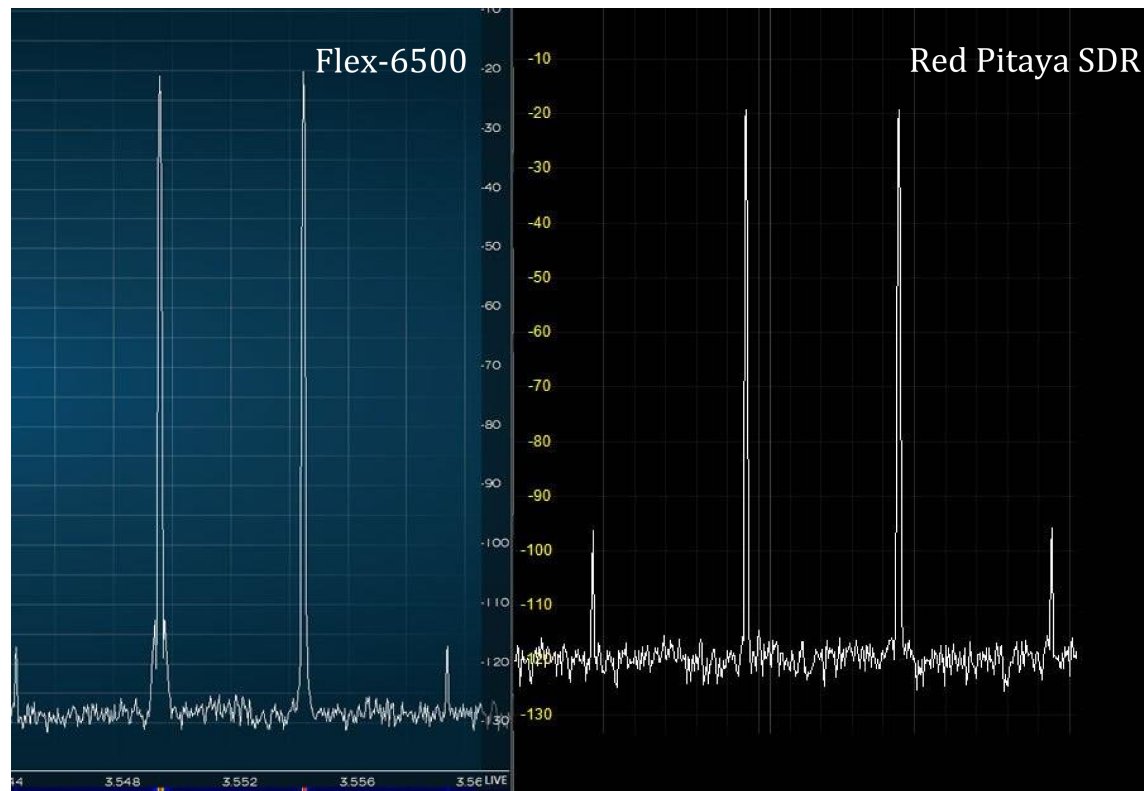
<http://www.mikrocontroller.net/topic/385102>



Comparison with Flex-6500

– Ger Metselaar (PA0AER) compared Red Pitaya SDR with Flex-6500:

<http://www.pa0aer.com/projecten/red-pitaya>



	Flex-6500	Red Pitaya SDR
Noise floor level	-130 dBm	-120 dBm
Suppression of the intermodulation products	97 dB	75 dB

Red Pitaya SDR in the news

– Johan van Dijk (PA3ANG) published an article about Red Pitaya SDR in the January, 2016 issue of DKARS Magazine:

<http://dkars.nl/index.php?page=magazine>

The image shows a screenshot of the DKARS Magazine website. The top part features the magazine's title "DKARS MAGAZINE" in large, bold, black letters on a yellow background. To the right is the DKARS logo, a diamond shape with a red top, yellow middle, and blue bottom, containing the text "DKARS". Below the title is a screenshot of the PowerSDR™ OpenHPSDR mRX PS v3.3.6 (11/16/15) software interface. The interface is dark-themed and displays various controls and data. A red circle is overlaid on the interface, containing the text "Red Pitaya SDR transceiver". The interface shows a frequency display of 3,630,000 Hz, a signal strength of -66 dBm, and a mode of 75M Extra SSB. The bottom part of the interface shows a spectrum display with various frequency bands and modes selected.

Concluding remarks

Summary

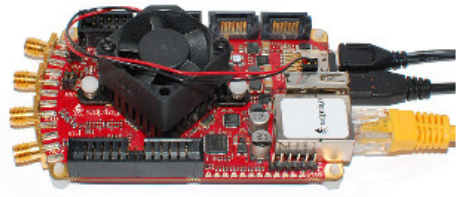
- Red Pitaya is a very interesting platform for building various measurement and control systems, experimenting with FPGA and DSP algorithms, sharing knowledge and experiences.
- It is a nice SDR building block thanks to the excellent open-source SDR tools.

Where is the source code?

– The source code and more details about my projects can be found at:

<http://pavel-demin.github.io/red-pitaya-notes>

Red Pitaya Notes Source Issues



1. List of components
2. Links
3. Development machine
4. LED blinker
5. SDR receiver
6. SDR transceiver
7. SDR transceiver compatible with HPSDR
8. SDR transceiver with FFT
9. Embedded SDR transceiver
10. Wideband SDR transceiver
11. Pulsed Nuclear Magnetic Resonance
12. Multichannel Pulse Height Analyzer
13. Scanning system
14. Debian with Red Pitaya ecosystem

Interesting links

- Red Pitaya

<http://redpitaya.com>

- The Scientist and Engineer's Guide to Digital Signal Processing

<http://www.dspguide.com>

- dspGuru: Digital Signal Processing Articles

<http://www.dspguru.com/dsp/articles>

- ARRL: Software Defined Radio

<http://www.arrl.org/software-defined-radio>

- GNU Radio: Suggested Reading

<http://gnuradio.org/redmine/projects/gnuradio/wiki/SuggestedReading>