Qucs
Quite Universal Circuit Simulator

Overview, Status and Roadmap

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Qucs /kjuːks/

• Overview
  – Project background
  – Package contents
  – What can you do with?
  – Demo

• Status
  – Development
  – Next release

• Roadmap
  – Our wishes for the future
Project background

- Started in 2003
  - Michael Margraf
  - Stefan Jahn
- GPLv2+
- 20+ contributors
- 20 languages
- Cross-platform
- Users
  - Education
  - Research
  - Hobbyists
  - Industry

- 2003 … 2016
- Qucs 0.0.18 - Windows

Web counter

DOWNLOAODS
1,184,765
In the selected date range

DOWNLOAODS
150,021
In the selected date range
Package contents

• (sort of an) IDE
• Schematic capture
• Simulation tools
  – Qucsator
  – Optimizer (ASCO)
  – Icarus-Verilog
  – FreeHDL
• Data visualization
• Equation system
• Component library
• Design / synthesis tools

• Extensible
  – Spice import
  – Verilog-A model builder
  – Octave/MATLAB

• Dependencies
  – C++ compiler
  – Qt4 (with Qt3Support)
  – Autotools / CMake
  – gperf / flex / bison
  – ADMS
  – LaTeX
Support

• Website
  http://qucs.sourceforge.net

• Current developers: ~ 6

• Documentation
  – Help
  – Tutorial Workbook
  – Report Workbook
  – Technical Manual

• SourceForge
  – Binaries
  – Git repository (mirror)
  – Issue tracker
  – Forum / mailing lists

• GitHub
  – Git repository (preferred)
  – Issue tracker
  – Wiki
  – Travis CI
  – AppVeyor
  – Coveralls
Tools

- Graphical Interface
  - Qucs
  - ActiveFilter
  - Attenuator
  - Editor
  - Filter
  - Help
  - Matching
  - Library
  - Rescodes
  - Transcalc

- ~ 170 components

- Command Line
  - qucs
  - qucsator
  - qucsconv

- Third-party and scripts
  - asco
  - admsXml
  - iverilog
  - freehdl
  - ps2sp
  - octave
  - python
Libraries

System Libraries
- Bridges
- Diodes
- Ideal
- JFETs
- LEDs
- MOSFETs
- NMOSFETs
- OpAmps
- PMOSFETs
- Regulators
- Substrates
- Transistors
- Varistors
- Z-Diodes

User Libraries
No User Libraries

RLC step transient simulation
- TR1
  - Type = lin
  - Start = 0
  - Stop = 3 us
  - Points = 1000

- V = 13.5 V
- L1 = 2 uH
- C1 = 450 pF
- R1 = 4 Ohm
- time = 0.5 us

Graph showing transient response v(t) vs. time (0 to 3e-6 s)
Visualization
Qucs-ActiveFilter (1)

Filter parameters:
- Passband attenuation, $A_p$ (dB): 3
- Stopband attenuation, $A_s$ (dB): 20
- Cutoff frequency, $F_c$ (Hz): 1000
- Stopband frequency, $F_s$ (Hz): 1200
- Passband ripple $R_p$ (dB): 3
- Passband gain, $K_v$ (dB): 0
- Filter order: 5

Transfer function and Topology:
- Approximation type: Butterworth
- Filter type: High Pass
- Filter topology: Sallen-Key (S-K)

General filter amplitude-frequency response:

Filter topology preview:

Filter calculation console:
- Filter order: 14
- Poles list $P_k = \Re + j\Im$
  - $-0.111964 + j0.993712$
  - $-0.330279 + j0.943883$
  - $-0.532032 + j0.846724$
  - $-0.707107 + j0.707107$
  - $-0.846724 + j0.532032$
  - $-0.943883 + j0.330279$
  - $-0.993712 + j0.111964$
  - $-0.993712 + j-0.111964$
Qucs-ActiveFilter (2)
Qucs-ActiveFilter (3)

Filter parameters:
- Transient bandwidth, TW (Hz): 3
- Stopband attenuation, As (dB): 20
- Upper cutoff frequency, Fu (Hz): 1000
- Lower cutoff frequency, Fl (Hz): 1200
- Passband ripple Rp(dB): 3
- Passband gain, Kv (dB): 0
- Filter order: 5

Transfer function and Topology:
- Approximation type: Butterworth
- Filter type: Band Stop
- Filter topology: Cauer section

General filter amplitude-frequency response:
- K (dB) vs. F (Hz)
- TW
- As

Filter topology preview:
- Diagram of the filter circuit

Filter calculation console:
- Filter order = 14
- Poles list Pk = Re + j*Im
  - -0.111964 + j*0.993712
  - -0.330279 + j*0.943883
  - -0.532032 + j*0.846724
  - -0.707107 + j*0.707107
  - -0.846724 + j*0.532032
  - -0.943883 + j*0.330279
  - -0.993712 + j*0.111964
  - -0.993712 + j*0.111964
Qucs-ActiveFilter (4)

Filter parameters
- Transient bandwidth, TW (Hz): 3
- Stopband attenuation, As (dB): 20
- Upper cutoff frequency, Fu (Hz): 1000
- Lower cutoff frequency, Fl (Hz): 1200
- Passband ripple Rp(dB): 3
- Passband gain, Kv (dB): 0
- Filter order: 5

General filter amplitude-frequency response

Transfer function and Topology
- Approximation type: Butterworth
- Filter type: Band Pass
- Filter topology: Sallen-Key (S-K)

Filter calculation console
- Filter order = 14
- Poles list: Re+j*Im
  - -0.111964 + j*0.993712
  - -0.330279 + j*0.943883
  - -0.512032 + j*0.846724
  - -0.707107 + j*0.707107
  - -0.846724 + j*0.532032
  - -0.943883 + j*0.330279
  - -0.993712 + j*0.111964
  - -0.993712 + j*-0.111964

Filter topology preview
Qucs-Attenuator (1)
Qucs-Attenuator (2)
Qucs-Attenuator (3)

Topography

Bridged Tee

Input

Attenuation: 1 dB
Zin: 50 Ohm
Zout: 50 Ohm

Output

R1: -- Ohm
R4: -- Ohm

Result:
Qucs is also a graphical user interface for performing digital simulations. This document should give you a short description on how to use it.

For digital simulations Qucs uses the FreeHDL program (http://www.frehdl.seul.org). So the FreeHDL package as well as the GNU C++ compiler must be installed on the computer.

There is no big difference in running an analog or a digital simulation. So having read the Getting Started for analog simulations, it is now easy to get a digital simulation work. Let us compute the truth table of a simple logical AND cell. Select the digital components in the combobox of the components tab on the left-hand side and build the circuit shown in figure 1. The digital simulation block can be found among the other simulation blocks. The digital sources $S_1$ and $S_2$ are the inputs, the node labeled as Output is the output. After performing the simulation, the data display page opens. Place the diagram truth table on it and insert the variable Output. Now the truth table of a two-port AND cell is shown. Congratulations, the first digital simulation is done!
Qucs-Matching
Qucs-Lib (1)

Component Selection

Diodes

1N4148
1N4148W
1N4148WS
1N4148WT
1N4001
1N4002
1N4003
1N4004
1N4005
1N4006
1N4007
1N5400
1N5401
1N5402
1N5404

Component

Name: 1N4148
Library: Diodes
universal silicon switching diode
75V, 300mA, 4.0ns
Manufacturer: Diodes Inc.

Symbol: ![Diode Symbol]

Paste into schematic

Copy to clipboard
Show Model
Qucs-Lib (2)
Qucs-Lib (3)

Component Selection

- Transistors
  - 2DA1774R
  - 2DC4617R
  - 2N2219A
  - 2N2222
  - 2N2222A
  - 2N2369A
  - 2N2484
  - 2N2905A
  - 2N2907
  - 2N2907A
  - 2N2955
  - 2N3019
  - 2N3053
  - 2N3055
  - 2N3280

Component

Name: 2DA1774R
Library: Transistors
universal silicon PNP BJT
50V, 150mA, 150mW, 140MHz
Manufacturer: Diodes Inc.
NPN complement: 2DC4617R
added by Leandro D'Archivio <morti667@hotmail.com>

Symbol:

! Drag n'Drop me !

Paste into schematic
Qucs-Rescodes

Paste into schematic

R1
R=47 Ohm
Qucs-Transcalc (2)
Qucs-Transcalc (3)

Transmission Line Type
- Grounded Coplanar

Substrate Parameters
- Er: 2.94
- H: 10 mil
- T: 0.1 mil

Physical Parameters
- W: 10 mil
- S: 5 mil
- L: 100 mil

Paste into schematic

S parameter simulation

Equation
- EqnTC1
- A = twoport(S, 'S', 'A')
- ZL = real(sqrt(A[1,2]/A[2,1]))

Ready.
Qucs-Transcalc (4)

Paste into schematic →

Transmission Line Type:
- Rectangular Waveguide

Substrate Parameters:
- Er: 1
- Mur: 1
- Cond: 4.1e+07
- Tand: NA

Physical Parameters:
- a: 1000 mil
- b: 500 mil
- L: 4000 mil

Equation:
- EqnTC2
  - A=twoport(S,'S','A')
  - ZL=real(sqrt(A[1,2]/A[2,1]))

Ready.
Qucs-Transcalc (5)

Transmission Line Type: Coplanar Waveguide

Substrate Parameters:
- Er: 2.94
- H: 10 mil
- T: 0.1 mil

Physical Parameters:
- W: 10 mil
- S: 5 mil
- L: 100 mil

Paste into schematic →

**Equation**

EqnTC1

A = twoport(S, 'S', 'A')
ZL = real(sqrt(A[1,2]/A[2,1]))

S parameter simulation

Ready.
Qucs-Transcalc (6)

Paste into schematic→

Transmission Line Type
- Microstrip Line

Substrate Parameters
- Er: 2.94
- Mur: 1
- H: 10 mil
- H_t: 1e+20 mil

Physical Parameters
- W: 9.99999 mil
- L: 99.999 mil

Equation
- EqnTC1
- A=twoport(S,'S','A')
- ZL=real(sqrt(A[1,2]/A[2,1]))

S parameter simulation
- SPTC1
  - Type=log
  - Start=0.1 GHz
  - Stop=10 GHz
  - Points=51

Ready.
Qucs-Transcalc

Transmission Line Type
- Coupled Microstrip

Substrate Parameters
- Frequency: 4.2 GHz
- NA: 0.88

Physical Parameters
- W: 0.219964 mm
- L: 25.4 mm
- S: 0.134874 mm
- Subst = SubstTC1
- er: 4.3
- h: 0.210058 mm
- t: 17.272 um
- tand: 0
- rho: 2.43902e-08
- D: 0

S parameter simulation
- Type: log
- Start: 1 GHz
- Stop: 100 GHz
- Points: 51

Paste into schematic →
Command Line Tools

- **Qucs** – schematic
  - schematic to netlist
  - schematic to print
  - dump components data

- **Qucsator** – simulator
  - DC
  - Transient
  - AC
  - AC Noise
  - S-Parameter
  - S-Parameter Noise
  - (Harmonic Balance)

- **Qucsconv** - converter
  - spice to qucs
  - spice to qucslib
  - vcd to qucsdata
  - qucsdata to csv
  - qucsdata to touchstone
  - citi to qucsdata
  - touchstone to qucsdata
  - csv to qucsdata
  - zvr to qucsdata
  - mdl to qucsdata
  - qucsdata to matlab

- **Custom file formats**
  - schematic
  - library
  - netlist
  - data file
Demo

• Examples
  – RLC circuit, parameter sweep
  – 555 timer: macro modeling
  – Optimization: Band-pass filter
  – 10 GHz microstrip band-pass filter
  – Verilog counter

• Development
  – Verilog-A support / model builder
  – Ngspice / Xyce front-end
RLC, parameter sweep

The voltage overshot strongly depends on the quality of the resonance circuit.

AC simulation
- **AC1**
  - Type=lin
  - Start=0.9 GHz
  - Stop=1.1 GHz
  - Points=150

Parameter sweep
- **SW1**
  - Sim=AC1
  - Type=log
  - Param=R_par
  - Start=1 Ohm
  - Stop=10 Ohm
  - Points=5

<table>
<thead>
<tr>
<th>number</th>
<th>R_par</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1.78</td>
</tr>
<tr>
<td>3</td>
<td>3.16</td>
</tr>
<tr>
<td>4</td>
<td>5.62</td>
</tr>
<tr>
<td>5</td>
<td>10.0</td>
</tr>
</tbody>
</table>

**Diagram:**
- Circuit diagram with voltage source, R1, L1, and C1.
- Graph showing voltage vs. frequency with parameter sweep results.
555 macro model

TR1
Type=lin
Start=0
Stop=0.6 ms
Points=1001
IntegrationMethod=Gear
Order=6
Maxiter=1500
reltol=0.01
abstol=100 pA
vntol=100 uV

C1
C=0.01u
V=0V

R1
R=3.9k

R2
R=3k

C2
C=0.01uF
V=0V

V3
U1=5 V
U2=0 V
T1=0
T2=0.02 ms
Tr=5 ns
Tf=5 ns

V1
U=5 V

vtrig

vout

reset

555
GND VCC
TRIG DIS
OUT TRESH
RES CON
SUB1

vdis

vout, Vt

0 1e-4 2e-4 3e-4 4e-4 5e-4 6e-4

5 0
Optimization (ASCO)

Equation

Eqn1
Left_Side_Lobe = max(dB(S[2,1]), 800e6:900e6)
Pass_Band_Ripple = min(dB(S[2,1]), 960e6:1040e6)
Right_Side_Lobe = max(dB(S[2,1]), 1100e6:1200e6)
S11_In_Band = max(dB(S[1,1]), 960e6:1040e6)

<table>
<thead>
<tr>
<th>number</th>
<th>Left_Side_Lobe</th>
<th>Pass_Band_Ripple</th>
<th>Right_Side_Lobe</th>
<th>S11_In_Band</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-23.1</td>
<td>-0.856</td>
<td>-22.7</td>
<td>7.47</td>
</tr>
</tbody>
</table>
Microstrip band-pass filter

10GHz band pass filter
Created by Toyoyuki ISHIKAWA

P1
Num=1
Z=50 Ohm

MS11
Subst=Subst1
W=384 um

MS1
Subst=Subst1
W=384um
L=5.24mm
S=482um

MS10
Subst=Subst1
W=384 um
L=1.08mm
S=712um

MS16
Subst=Subst1
W=1.08mm
W2=384um

MS6
Subst=Subst1
W=1.08 mm

MS17
Subst=Subst1
W=1.08mm
W2=1.3mm

MS7
Subst=Subst1
W=1.3mm

MS18
Subst=Subst1
W=1.08mm
W2=1.3mm

MS8
Subst=Subst1
W=1.08 mm

MS19
Subst=Subst1
W=1.08mm
W2=384um

MS20
Subst=Subst1
W=384 um
L=5.24mm
S=482um

MS13
Subst=Subst1
W=1.3mm
L=5.03mm
S=913um

MS14
Subst=Subst1
W=1.08mm
L=4.72mm
S=712um

MS15
Subst=Subst1
W=384um
L=5.24mm
S=482um

S parameter simulation
SP1
Type=lin
Start=5 GHz
Stop=15 GHz
Points=150

Equation
Eqn1
dB_S21=dB(S[2,1])
dB_S11=dB(S[1,1])

P2
Num=2
Z=50 Ohm

Subst1
er=2.56
h=0.76 mm
t=18 um
tand=3e-3
rho=0.022e-6
D=100
Verilog Counter

module counter(out, clk, reset);

parameter WIDTH = 2;

output [WIDTH-1 : 0] out;
input           clk, reset;

reg [WIDTH-1 : 0] out;
wire           clk, reset;

always @(posedge clk)
  out <= out + 1;

always @(reset)
  if (reset)
    assign out = 0;
  else
    deassign out;

endmodule // counter

Verilog simulation with Icarus Verilog
Check the 'counter.v' for the HDL model.
Verilog-A

• Includes 53-38 models written in Verilog-A

• Compact models
  – BSIM 3, 4, 6 (Berkeley)
  – EKV (EPFL)
  – HICUM L0, L2 (TU-Dresden)
  – FBH-HBT (TU-Berlin)

• ADMS (Automatic Device Model Synthesizer)
  – Verilog-A → XML transformations → “XYZ code”

• Limitations
  – Subset of Verilog-AMS
  – Not supported: $V(n)<> … ;$

CMC license issues

Accellera license issue
Verilog-A model builder

- BSIM6: Qucsator x HSPICE
spice4qucs: Ngspice / Xyce

- Audio amplifier, troubles with Qucsator
Status

• Release 0.0.19 (February 05, 2016)
  – Bug fixing, usability improvements, build system cleanup
  – Ongoing port Qt3Support to Qt4
  – New active-filter synthesis tool
  – Integration of regression tests, qucs-test repository
  – Removal of non-GPL models
  – ...

• Release 0.0.20 (no due date)
  – BSIM 6
  – New RF models
  – spice4qucs: Ngspice (XSPICE) and Xyce frontend
    • https://github.com/Qucs/qucs/issues/77
    • https://github.com/ra3xdh/qucs/releases/tag/0.0.19S-rc3
  – Tuner, Gnu-cap/Gnu-csator, make ADMS optional, submit package to Debian, multiple simulators…
Roadmap (wish list)

1. Simple GUI and simulator
   – Refactor/rewrite, (Qt4) Qt5, plug-ins, API…
   – Standard file formats, exchangeable
2. Powerful circuit analysis tools
   – Robust algorithms (Eigen, KLU)
   – API, high level interface (SWIG)
   – Harmonic-Balance
   – Large signal S-parameter simulation (LSSP)
   – EM field simulation / extraction (openEMS, NEC2++)
   – *SPICE flavors compatibility/converter
   – Co-simulation (analog + Verilog/VHDL), interface (icarus, GHDL)
   – Monte-Carlo simulation
   – Solvers: Ngspice, Xyce, Gnucap, SpiceOpus
3. Design and synthesis tools
   – Data import / export
4. Industry standard device models
   – MEXTRAM, VBIC, HiSIM, IGBT, UTSOI, …
5. Hardware implementation
   – Layout PCB, device (KiCad, Klayout)
Resources

- Website: http://qucs.sourceforge.net/
- GitHub (preferred): https://github.com/Qucs/qucs/
- SourceForge: http://sourceforge.net/p/qucs/git/
- Mailing lists: http://sourceforge.net/p/qucs/mailman/
- IRC channel: #qucs
- Forum: http://sourceforge.net/p/qucs/discussion/
- Bug trackers:
  - https://github.com/Qucs/qucs/issues
  - http://sourceforge.net/p/qucs/_list/tickets
- Source code documentation:
- Downloads: http://sourceforge.net/projects/qucs/files/
- (NEW) Qucs-Help: http://qucs-help.readthedocs.org/
- (NEW) Transifex translations:
Final remarks

• Flexible and easy to use
• Advanced components and features
• Build and test infrastructure
• Right time for refactoring/redesign
• We are open for collaboration
• Roadmap: Your help is welcome!