

A decorative graphic on the left side of the slide, consisting of a network of light blue lines and circles that resemble a circuit board or a data network. The lines are vertical and horizontal, with some diagonal connections, and the circles are of varying sizes, some acting as nodes or junctions.

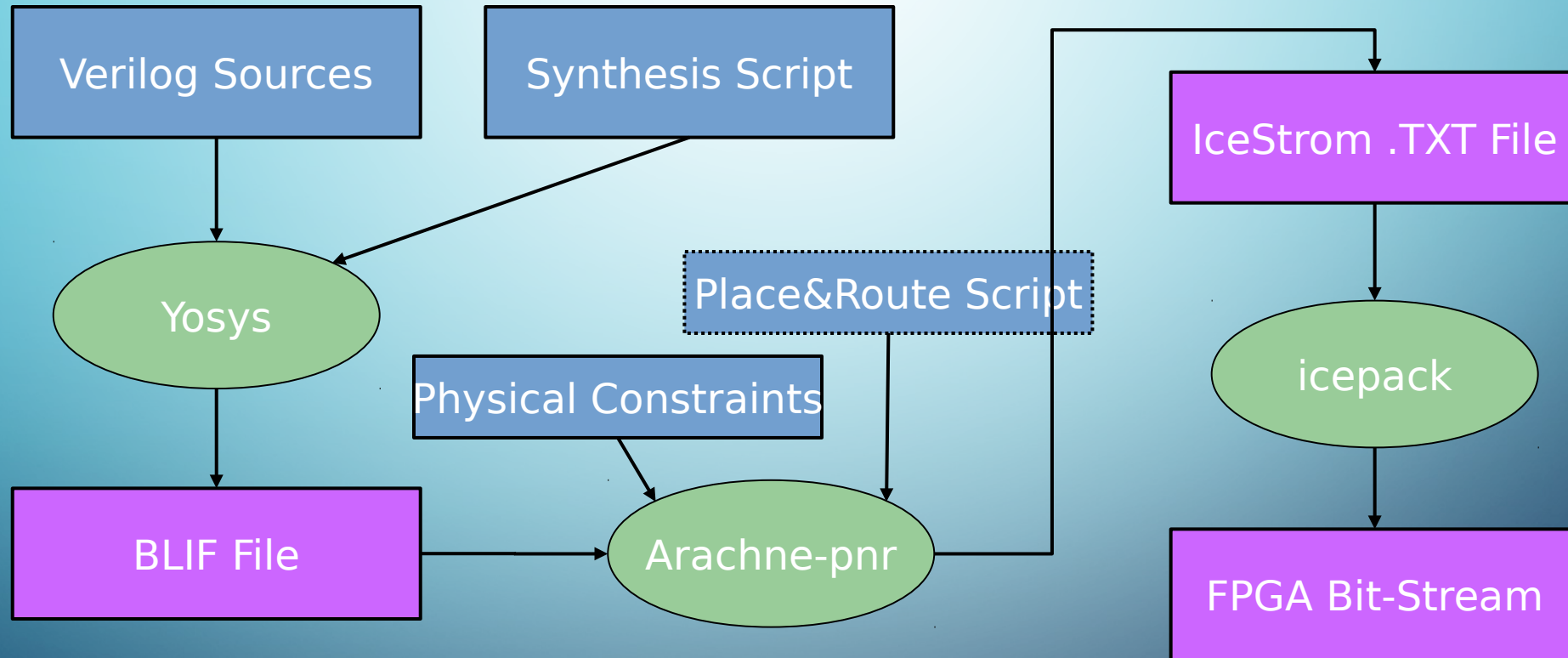
OPEN SOURCE FPGA TOOLCHAIN

WHY IF VIVADO AND QUARTUS ARE „FREE“ ANYWAY

WHOAMI

- Open Source Evangelist
- Team: Clifford Daniel Edmund

WHAT DO WE HAVE: FPGA TOOLCHAIN



	Yosys Arachne-pnr	Synplify Pro SBT Backend	Lattice LSE SBT Backend
Packed LCs	2996	2647	2533
LUT4	2417	2147	2342
DFF	1005	1072	945
CARRY	497	372	372
RAM4K	8	7	8
Synthesis Time	30 seconds	30 seconds	21 seconds
Implementation Time	81 seconds	405 seconds	415 seconds

Design	Timing Tool	Yosys Arachne-pnr (unconstrained)	Lattice LSE SBT Backend (constr. 100 MHz)
PicoRV32_AXI (w/ reduced pin count)	sbttime	N/A	41.74 MHz
	icetime -i	54.33 MHz	41.75 MHz
	icetime -im	53.02 MHz	41.40 MHz
Navre AVR Clone (from Milkymist SoC)	sbttime	N/A	45.82 MHz
	icetime -i	29.89 MHz	45.59 MHz
	icetime -im	27.61 MHz	44.90 MHz
Whishbone SPI Core (from OpenCores)	sbttime	N/A	62.13 MHz
	icetime -i	42.62 MHz	62.23 MHz
	icetime -im	38.89 MHz	61.14 MHz

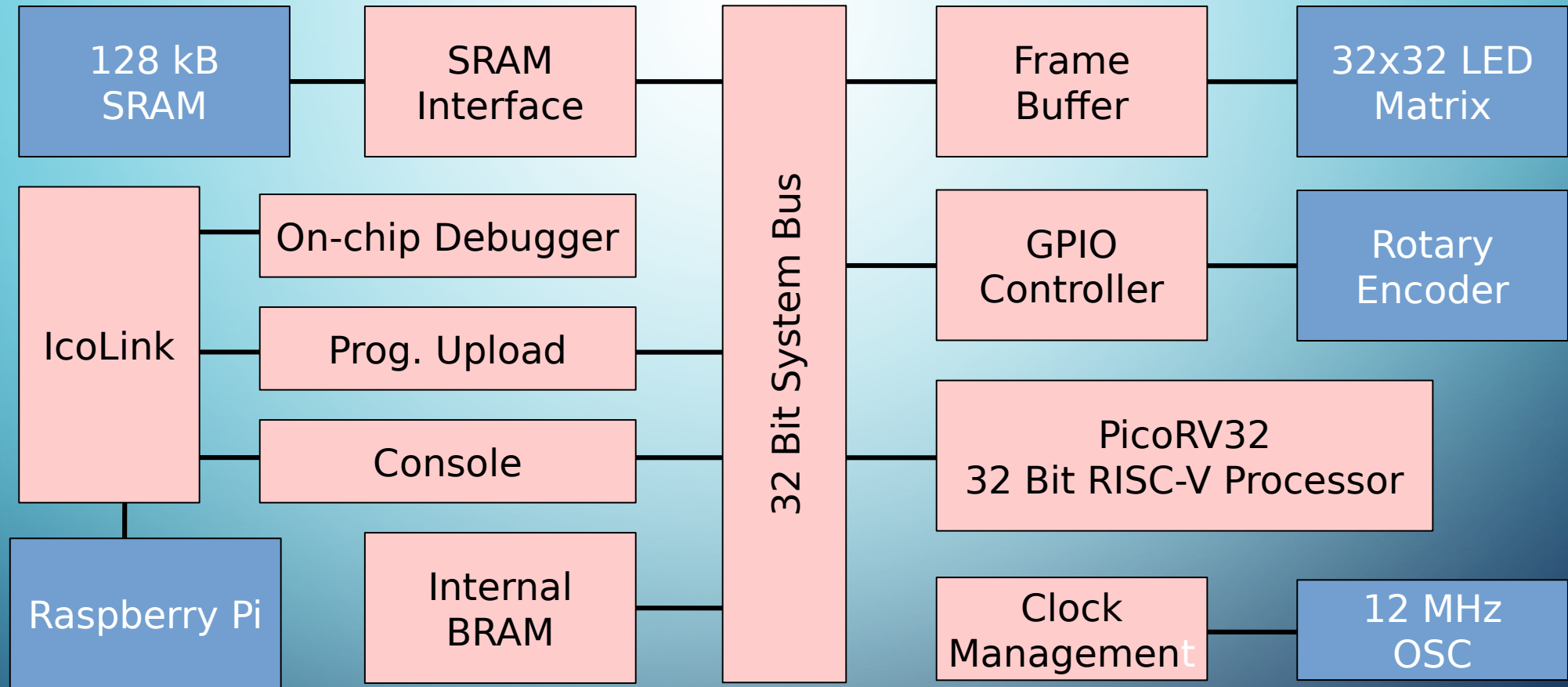
WHAT DO WE HAVE: BOARDS

- Lattice ICEstick 1k (21 USD)
- Lattice evaluation board 8k LUT (42 USD)
- IcoBoard 8k LUT , 1 Mb SRAM, Flash (90 Euro)
- Olimex, BQ

WHAT DO WE HAVE: Verilog IP BLOCKS

- CPUs
- SRAM, SPI, UART, I2C, ...
- Minimal Risc-V SoC

Demo SoC - Simplified Block Diagram

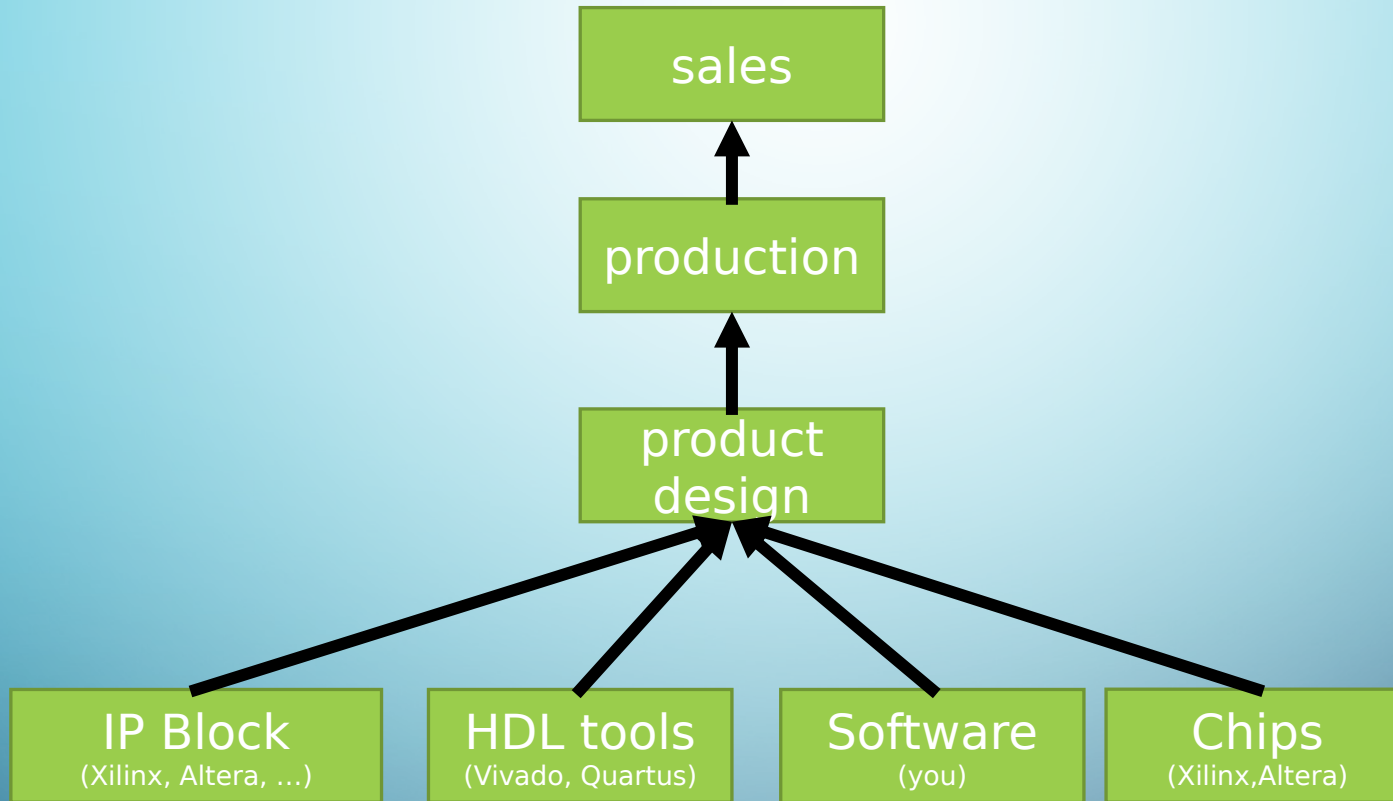


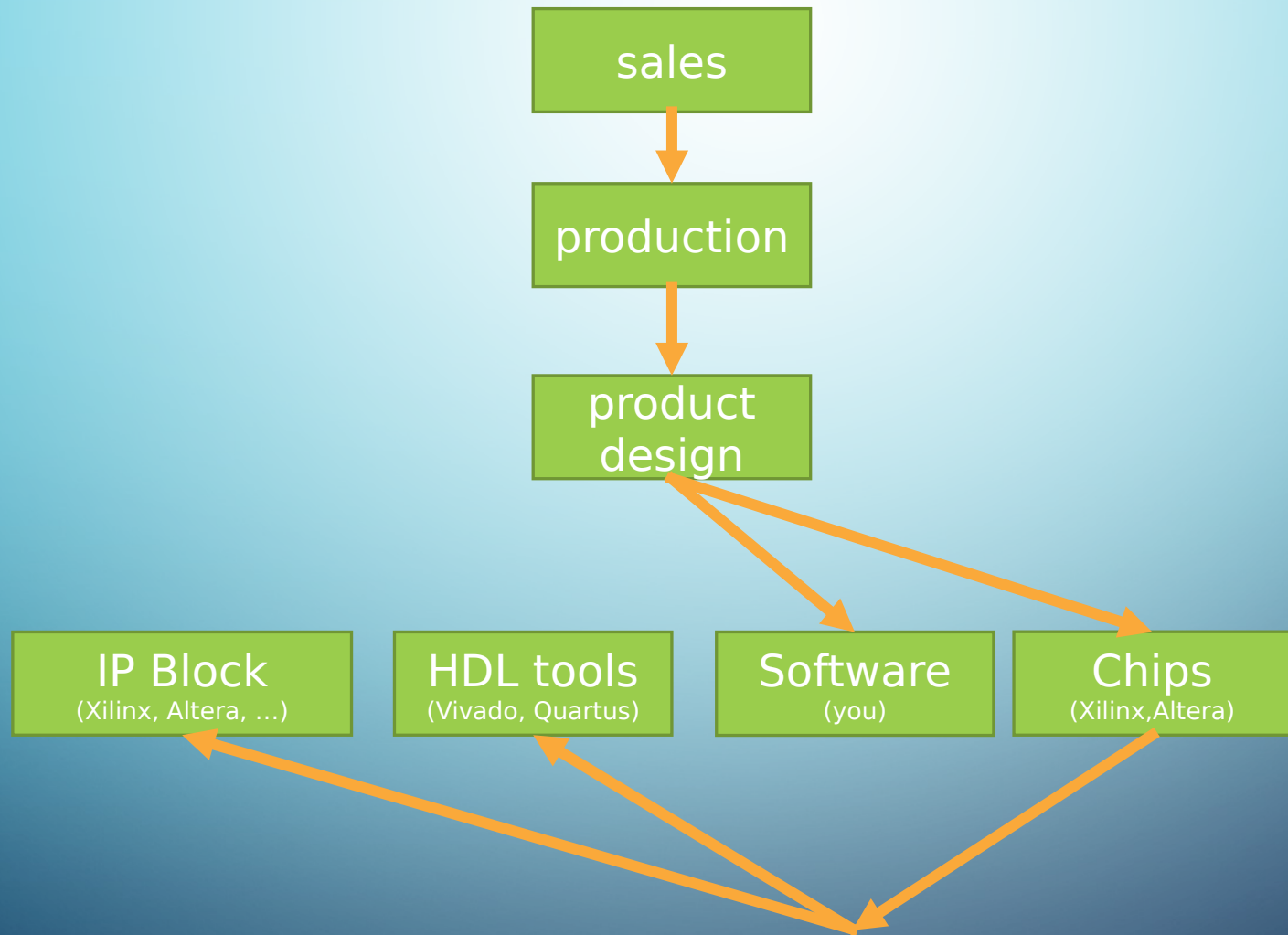
OPEN SOURCE TOOLCHAIN: WHY CARE?

- learning
- innovation
- Integration
- wastefull IP

The background is a blue gradient with decorative white circuit-like lines in the corners. The lines consist of straight segments and small circles, resembling a printed circuit board or a network diagram. They are located in the top-left, top-right, bottom-left, and bottom-right corners.

The Industry





The background is a blue gradient with decorative white circuit-like lines in the corners. The lines consist of straight segments and small circles, resembling a printed circuit board layout. They are located in the top-left, top-right, bottom-left, and bottom-right corners.

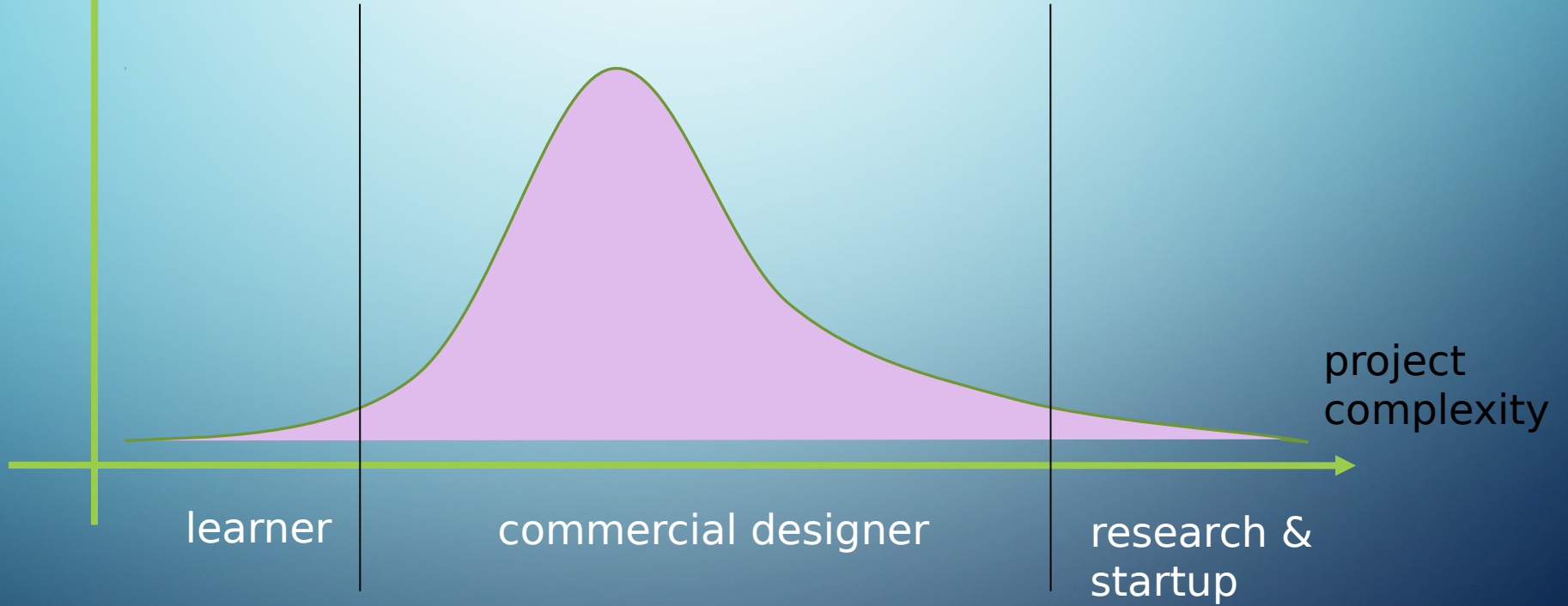
GOAL:

make money by moving many chips

number of chips sold

„we make tools for the guys who move chips“

„design win!“






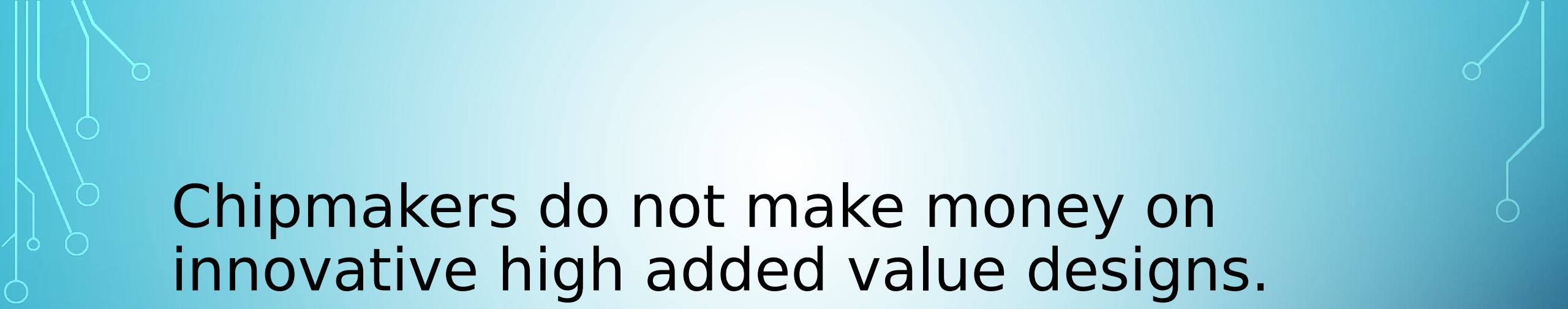


Learners dont buy many chips

==> manufacturer do not
listen/invest in their requirements

tools are too powerfull
tools are too complicated





Chipmakers do not make money on innovative high added value designs.



Innovators only move small number of chips

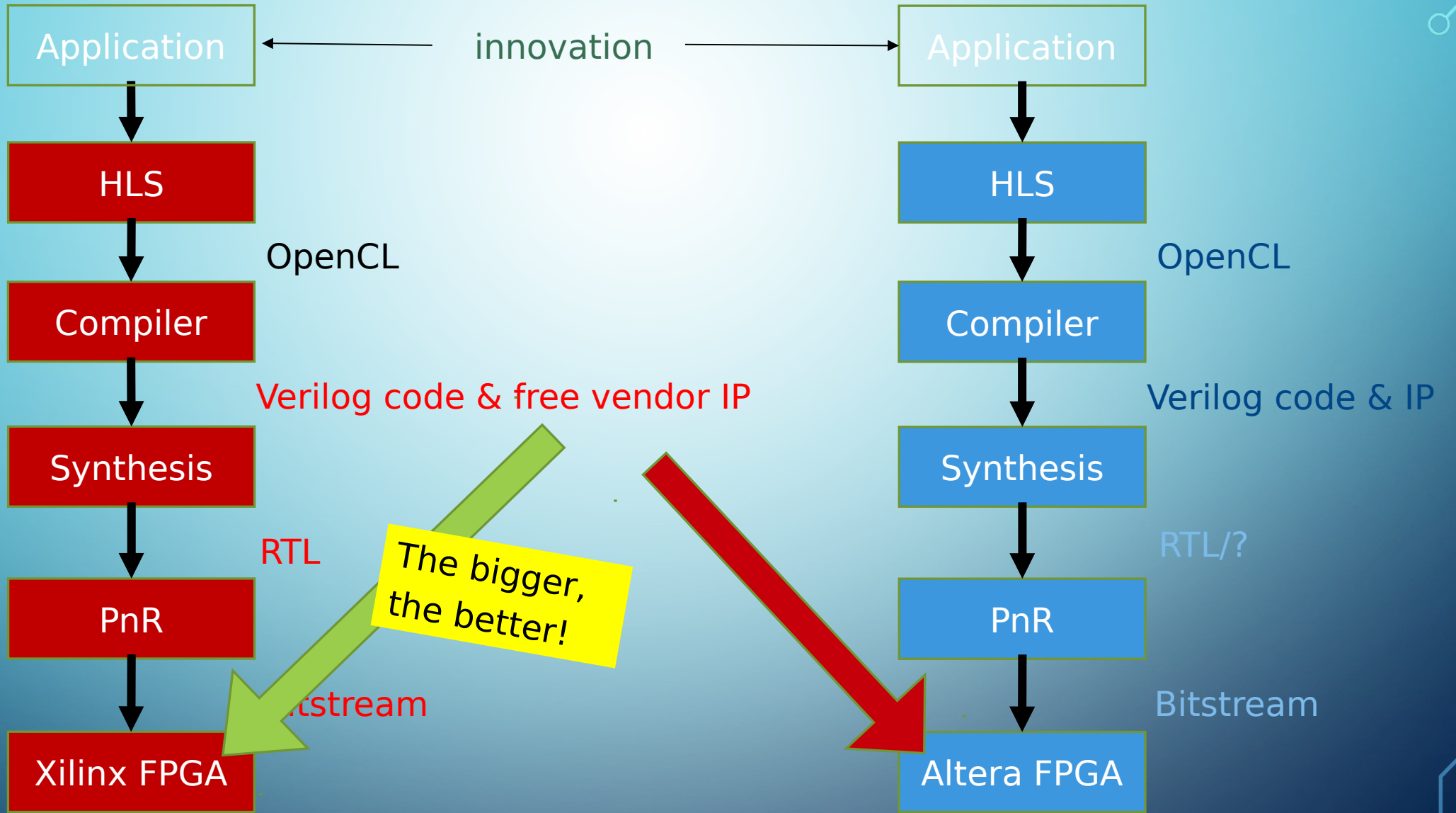
==> no good toolsupport for innovation






→ LITTLE TOOL INNOVATION

- No new programming tools
(Verilog was started 1984, Perl was started 1987)
 - No new usecases (which usually start out small)
 -
- 
- 

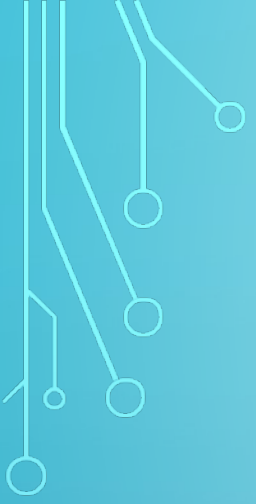


- 
- makes cross vendor integration hard and expensive
 - Is In the interest of Altera and Xilinx
 - They love „lock in“, not sharing, reuse and innovation




The background is a blue gradient with decorative circuit board patterns in the corners. The patterns consist of white lines and circles, resembling traces and vias on a PCB. The top-left and bottom-left corners have more complex, branching patterns, while the top-right and bottom-right corners have simpler, more linear patterns.

Green walled gardens of Xilinx and Altera.

Think „Unix wars“



For an innovation very often you have to touch the whole stack

- If a part of stack is propriety, this component determines the speed of innovation.
 - With open compenents, innovation can go forward faster.
 - There would be no Facebook without Linux.
- 
- 
- 

Applikation

IDE

Yosys

Arachne

ICE40 FPGA

innovation

Verilog

RTL

bitstream

Application

HLS

Compiler

Synthesis

PnR

Xilinx FPGA

Applikation

Integration IDE

Yosys

Arachne

ICE40 FPGA

Application

HLS

Compiler

Synthesis

PnR

Altera FPGA

OpenCL

OpenCL

Verilog code & IP

Verilog modules

Verilog code & IP

RTL

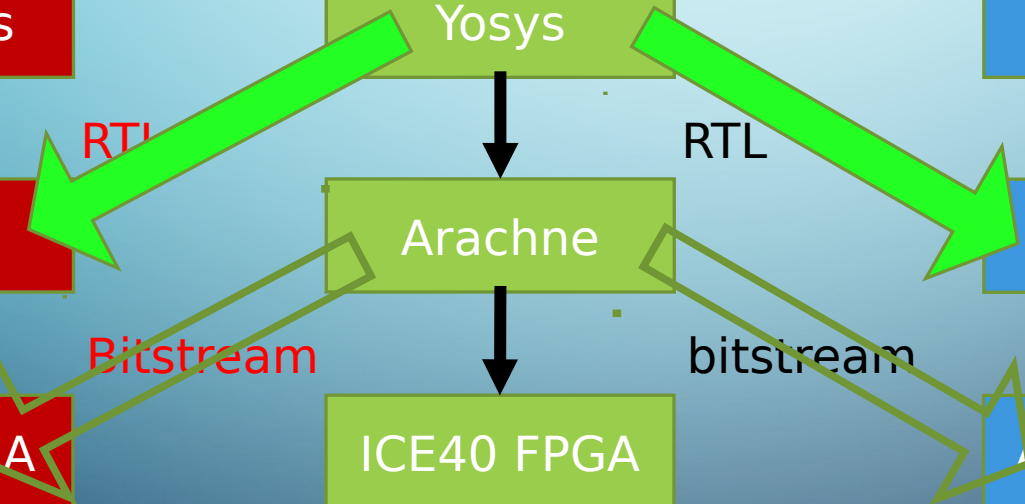
RTL

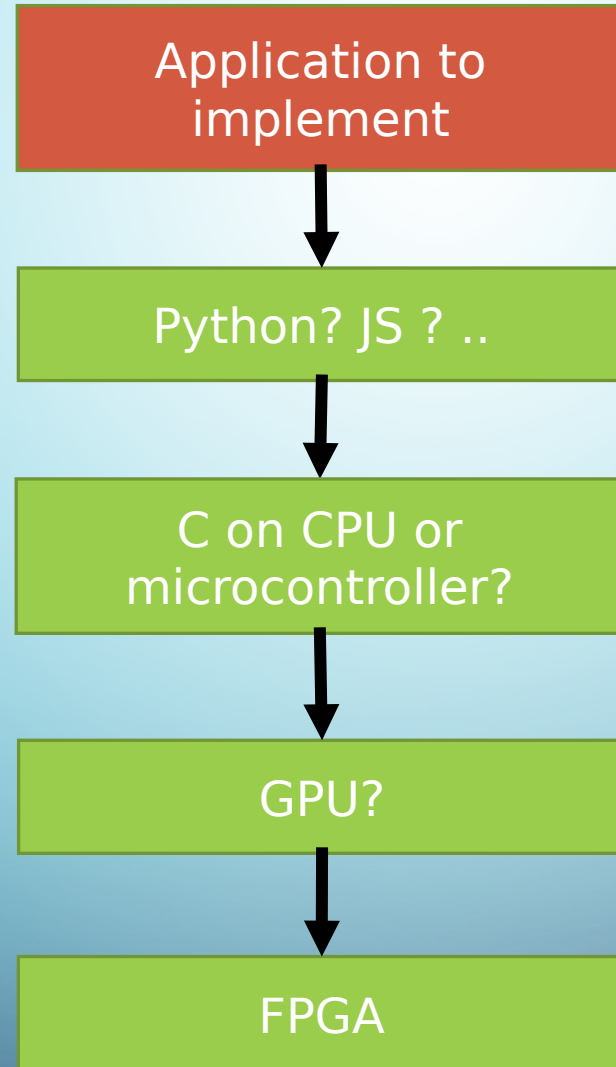
RTL/?

Bitstream

bitstream


Bitstream





FPGA is hard!

Use it only if you need to!

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- The background features a blue gradient with white circuit-like lines in the corners. These lines consist of straight paths that branch out and terminate in small circles, resembling a network or data flow diagram.
- Application has requirement for low latency
- Application has a huge bandwidth-requirement and a streamable solution
- Application has requirement for precise timing

USECASES for Lattice ICE40

- digital design education
- research
- control-systems
- dynamic trigger in logic analyser
- signal predistortion, fast sensordata processing
- ...
- embedded bitstream generation

We are looking ...

- to grow the eco system
- to write open/free Verilog blocks
- to have great demo usecases
- to support larger/faster FPGAs
- for learners and innovators
- to develop an integrated IDE to ease integration

The slide features a blue gradient background with decorative white circuit board traces in the corners. The traces consist of lines and circles, resembling a PCB layout. The top-left and bottom-left corners have more complex, branching patterns, while the top-right and bottom-right corners have simpler, more linear traces.

More technical presentation:

Clifford Wolf: Author of Yosys

AW1.121 EDA developer room today 14:00

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Q & A ...

<http://icoboard.org>