Digital Hardware Design
Why is it still so hard?

Philipp Wagner

LibreCores
Free and Open Digital Hardware
www.librecores.org

FOSSi
Foundation

The story of Ton Lear

The story of Not Real

What's the difference?

Digital Hardware Design

maker

Free and Open Source Silicon (FOSSi)

open (source) hardware

FOSSi Reality Check 1

The Simulation Check

Simulation: Required Ingredients

- code to simulate
- a simulator
- testing

Write your code

- Choose from the incumbents
  - Verilog/SystemVerilog
  - VHDL
- or one of the new contenders
  - Bluespec SystemVerilog
  - Chisel (UC Berkely)
  - MyHDL

Simulation

- The “big 3” commercial simulators
  - Incisive Enterprise Simulator/ NCSim (Cadence)
  - ModelSim (Mentor)
  - VCS (Synopsys)
- FOSS solutions
  - Icarus Verilog
  - GHDL
  - Verilator
- Add a good waveform viewer
  - gtkview

Testing & Verification

- cocotb: Python-based test
- vunit: VHDL unit testing
- Open Source VHDL Verification Methodology (OS-VVM)

“The Simulation Check”: Results

- Hobbyist-Accessibility-Score: 4/5
- FOSS score: 4/5
- Fun score: 2/5

FOSSi Reality Check 2

The FPGA Check

FPGA Design: Required Ingredients

- code to simulate
- a simulator
- testing
- a synthesis tool
- an implementation tool
- an FPGA board

FPGA Synthesis

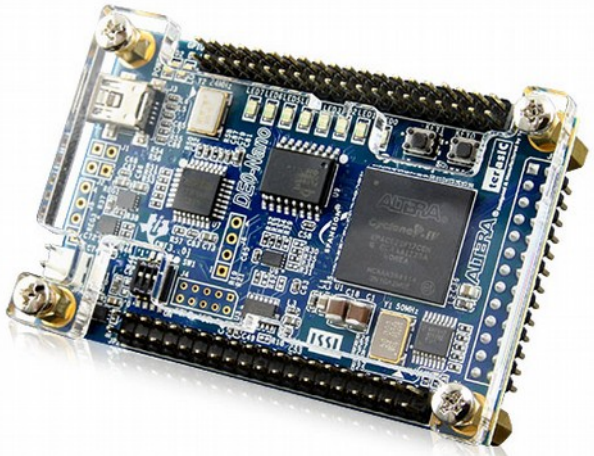
- Commercial
  - Synopsys Synplify
  - vendor tools (Xilinx, Altera, …)
- free alternatives
  - Verilog-to-Routing (VTR)
  - Yosys

FPGA Implementation

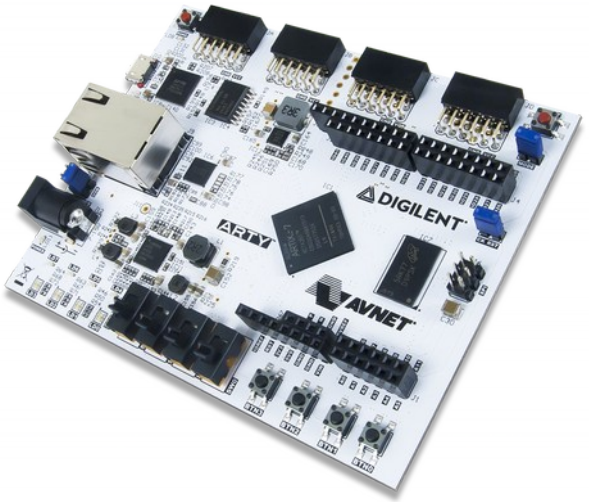
- Mostly vendor tools
  - Xilinx ISE/Vivado, Altera Quartus, …
- free alternatives
  - IceStorm for Lattice iCE40
    watch Clifford's presentation in the EDA Devroom today at 14:00

FPGA Boards: student (< 100 $)

iCEstick
$20
1280 cells



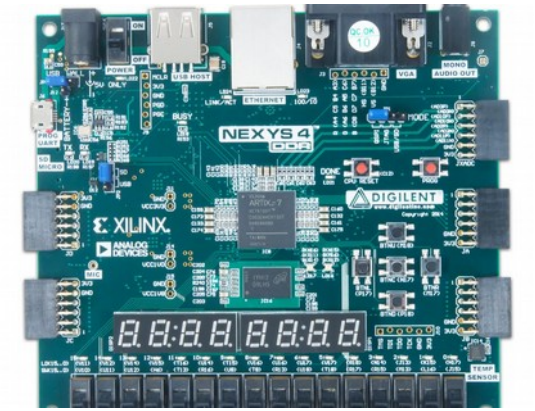
DE0-Nano
$79
22,320 cells



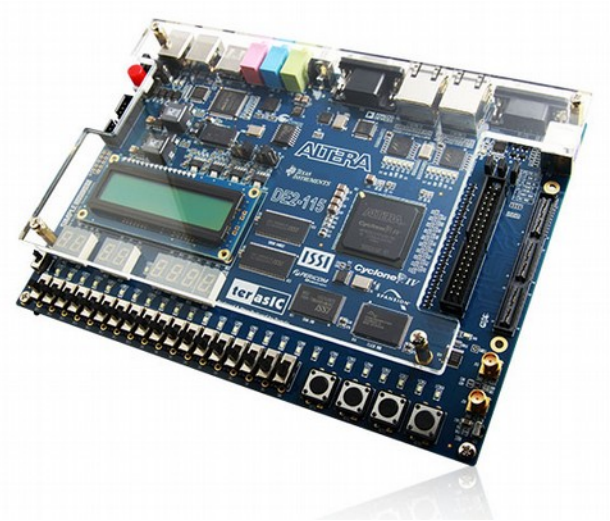
Artix-7 35T
$99
33,280 cells

All board pictures (c) by the manufacturers.

FPGA Boards: amateur (~ 500 $)



Nexys 4 DDR

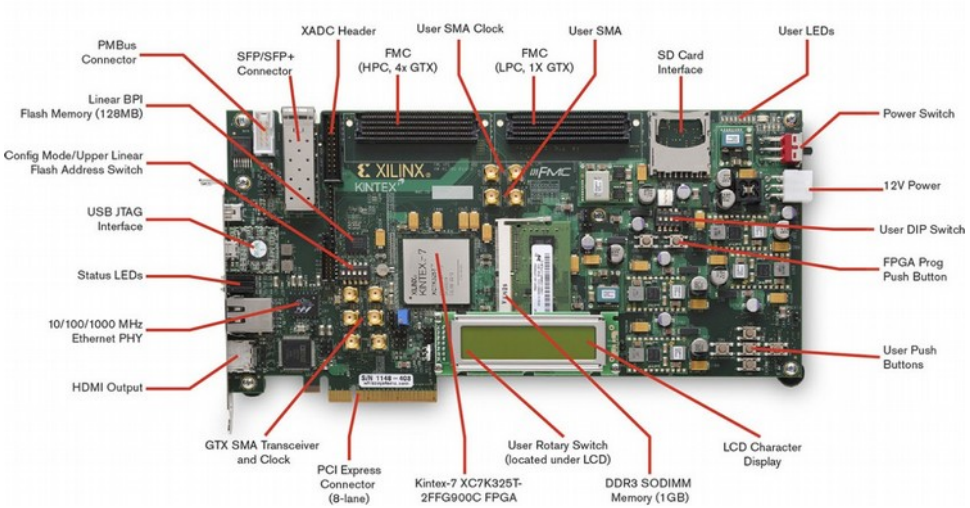


Altera DE2-115

ZTEX 2.1x

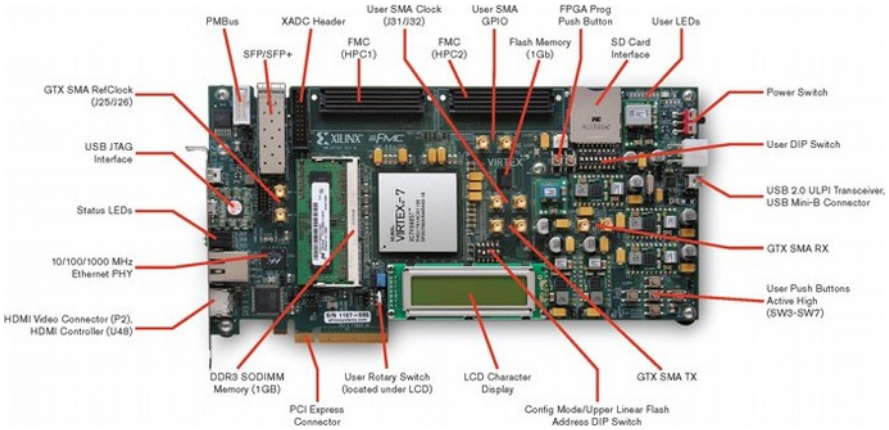
All board pictures (c) by the manufacturers.

FPGA Board: pro (> 1000 $)



Xilinx KC705

Altera Cyclone V SoC Development Kit



Xilinx VC707

All board pictures (c) by the manufacturers.

“The FPGA Check”: Results

- Hobbyist-Accessibility-Score: 3/5
- FOSS score: 2/5
- Fun score: 4/5

FOSSi Reality Check 3

The ASIC Check

ASIC Production: Required Ingredients

- code to simulate
- a simulator
- a synthesis tool
- really good testing & verification
- a design kit
- an implementation tool
- money

The Design Kit

- standard cell libraries, design rules, electrical parameters, ...
- get it from the foundry
- bad: requires pretty tough NDA
- good: it's usually for free (again, as in beer)

ASIC Implementation

- Commercial options
  - Synopsys Design Compiler
  - Cadence Encounter Toolset
- FOSS options
  - qflow
  - Coriolis2

Got Money?

[[user:]] via Wikimedia Commons, CC BY-SA

Need Money

- Multi-Project Wafer
  - available from multiple vendors, e.g. Europractice
  - example
    - 50 pcs Globalfoundries 40 nm
    - 4 750 €/mm² (at least 9 mm² = 42 750 €) + packaging, etc.
    - up to 1500 KGates/mm²
  - cheaper in older technologies (65nm + up)
- eASIC
  - pre-characterized ASICs “configured” with one custom layer

“The ASIC Check”: Results

- Hobbyist-Accessibility-Score: 0.1/5
- FOSS score: 1/5
- Fun score: 1-5/5
- Satisfaction score: 10/5

let's do it anyways?

Don't celebrate alone.

Picture by Wei-chieh Chiu (flickr), CC BY-SA

Join the party!

The bachelor party. Signed Louis Wain. Oil on canvas, 29.5 x 60 cm (public domain, via Wikimedia Commons)

FOSSi Reality Check 4

The Community Check

Required ingredients

- Let others participate
- Build on existing work
- Learn, teach and exchange ideas

How to live together?

photo by Prskavka (Wikimedia Commons), public domain

Let others participate, part 1: choose a license

- Permissive
- Weak Copyleft
- Strong Copyleft

Licensing: Permissive

- without patent clause
  - MIT and BSD widely used
  - example project: RISC V
- with patent clause
  - new: SolderPad License by Andrew Katz

Licensing: Weak Copyleft

- File-based copyleft
  - OHDL: Julius Baxter for mor1kx, based on MPLv2
- library copyleft
  - LGPL
    - commonly used on opencores.org
    - what's “linking” in a hardware context?

Licensing: Strong Copyleft

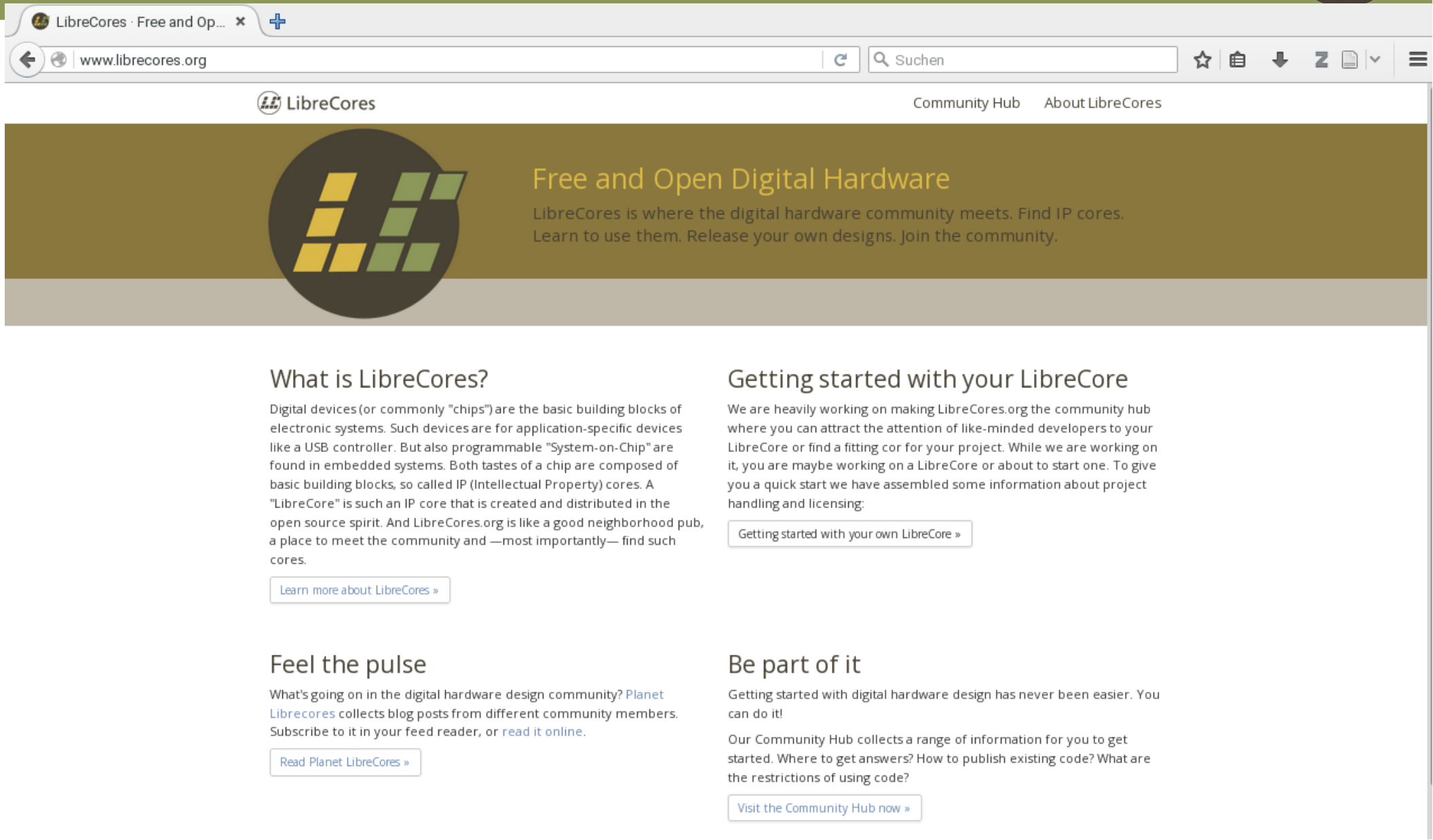
- GPL
  - GPLv3 uses “hardware-friendly” language
    - lesson learned from open sourcing SPARC
  - example user: Gaisler LEON3 (GPLv2+)
  - implications not fully understood
    - ASIC (design kit)?
    - FPGA (built-in primitives)?

photo by Andre Glechikoff (Flickr), CC BY-SA

Community hub needed

- publish your work
- find code to re-use
- learn, teach, inspire

Introducing LibreCores



LibreCores Goals

- Documentation
  - How to get started?
  - Best practices
  - Success stories
- News & Discussion
  - Planet LibreCores
- Project repository
  - a directory of FOSSi projects
  - with quality indicators

LibreCores: Where are we today?

- Documentation
  - How to get started?
  - Best practices
  - Success stories

First content online as of today

- News & Discussion
  - Planet LibreCores

online!

- Project repository
  - a directory of FOSSi projects
  - with quality indicators

coming soon

Who's behind all that?

- OpenRISC community
- Group formed ~2 years ago
- First plans presented at ORCONF 2015 at CERN
- since end of 2015: FOSSi Foundation, CiC (UK) to provide shared legal entity

So: Why is it still so hard?

- you can do your own simulated and FPGA design today!
- producing ASICs will remain a challenge

But mostly:
It's hard because information is hard to find.
LibreCores is ready to change that. Join us!

Peter Falk (by Sten), photo by Emanuele (flickr), CC BY-SA

TheOpenCorps!

The Open Corps | Home | Docs | Plans | Search theOpenCorps | Sign in with GitHub

RTL design for the 21st century.

We're a friendly collection of developers helping to improve FPGA design.

- Automated regressions using **Travis-ci**
- Host your code on **GitHub**
- Synthesise using **Quartus** and **Vivado**
- Simulate with **Riviera-PRO**

Sign up for free!

Latest Projects

	Project	Description	Docs	Simumlation	Synthesis	
☆	JPEG Encoder	Convert raw bitmap images into JPEG files	docs passing	tests 43 passing	Xilinx 130MHz	Altera 170MHz
☆	Base-10 Logarithm	Perform base10 logarithm arithmetic	docs passing	tests 1 passing	Xilinx 210MHz	Altera 180MHz
☆	DVB-S2 LDPC Decoder	Convert raw bitmap images into JPEG files	docs passing	tests 12 passing	Xilinx 100MHz	Altera 300MHz
☆	Huffman Decoder	Decode huffman trees (used in compression)	docs None	tests None	Xilinx 120MHz	Altera 120MHz
☆	Parallel CRC Generator	Create CRC on multiple bits per clock cycle	docs passing	tests 43 passing	Xilinx 130MHz	Altera 170MHz

Latest Activity

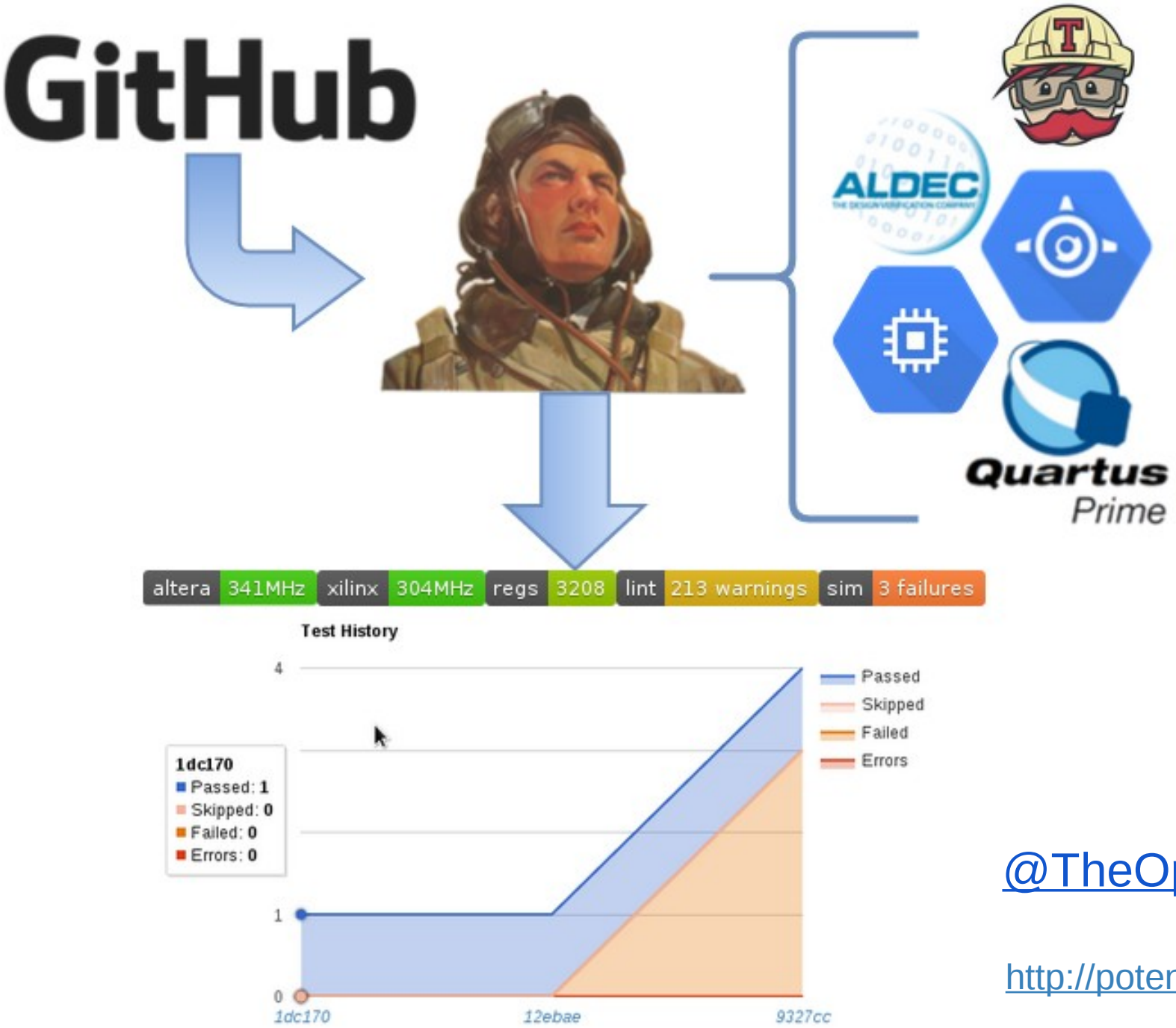
POTENTIAL VENTURES

TheOpenCorps: Goals

- Provide status indications for HW projects
  - Does it build?
  - Does it have sims / do they pass?
  - Resource utilisation and frequency
- Improve quality of Open Source HW
- Encourage re-use in Open Source HW
- Free access to proprietary tools

TheOpenCorps: Flow

- Code hosted on Github
- Describe build using .opencorps.yml
- Develop!
- For each commit:
  - Simulation regression
  - Synthesis on multiple platforms
- Report status



@TheOpenCorps

http://potential.ventures

POTENTIAL VENTURES

let's talk!

FOSSi Foundation

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